# Fabrication and characterization of silicon nanowires with triangular cross section

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Fabrication processes for silicon nanowires with triangular cross section are presented. Processes based on high resolution electron beam lithography and anisotropic etching have been developed on silicon on insulator substrates. As shown by numerical simulations, the triangular shape of the wire allows strong reduction of the dimensions by successive oxidation steps. Moreover, it is easy to define a gate on top of the wire that wraps the device and, with the back gate silicon substrate, allows the biasing of the structure on all sides. The conduction through the wire, as a function of the gate bias and for different temperatures, is reported and discussed. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2338599]

## I. INTRODUCTION

The increasing complexity of electronic systems is stimulating research in developing fabrication technologies for smaller and more efficient devices. Owing to the decrease of device dimensions, electrons are forced in spaces comparable with their wavelength and effects have begun to be investigated. This has also caused more interest in developing technologies for the realization of structures with dimensions in the nanometric range. In the past years several devices with nanometric dimensions have been fabricated by using electron beam lithography and compound semiconductors, such as GaAs, exploiting high mobilities of bidimensional electron gases. The diffusion of silicon technologies for integrated circuit fabrication is stimulating the development of processes for silicon based nanostructure. Silicon nanowires have been fabricated by means of several techniques, including the bottom-up approach such as chemical vapor deposition[1–5] and the top-down nanoscale definition.[6–9] Most of the proposed top-down techniques are based on high resolution electron beam (e-beam) lithography and reactive ion etching (RIE) for defining devices on the top silicon layer of a silicon on insulator (SOI) wafer. Silicon nanostructure on SOI wafers have also been fabricated by alternative methods based on both different lithographic tools and different silicon etching techniques. As far as lithography is concerned, atomic force microscopy (AFM) methods have been successfully used[10–12] and silicon nanowire have also been fabricated by conventional optical lithography providing a suitable design and orientation of the mask.[13,14] Electrochemical[15] and anisotropic silicon etchings[10,11,14,16] have been proposed as alternatives to the RIE etching. Silicon wires have been investigated not only for their transport characteristics or as building blocks for more advanced and complex nanoelectronic devices, as silicon single electron transistors,[17,18] but also for other application fields such as biological[19] and nanomechanical[20] sensors.

The aim of this work is to present fabrication processes for silicon nanowires with triangular cross section that can be efficiently reduced by thermal oxidation, as confirmed also by numerical simulations. The grown oxide layer can be employed as insulator for a gate that, due to the particular obtained geometry, wraps the wire all around. Electrical conduction has been studied in low doped silicon wires, and measurements show that conduction is driven by inversion layers generated at the corners of the triangular section, in agreement with electrostatic numerical simulations.

## II. STRUCTURE DESCRIPTION

The proposed processes for silicon wire fabrication, described in detail in the next section, are based on silicon anisotropic etching (in the specific case KOH etching), applied to features defined by electron beam lithography on SOI substrate ⟨100⟩ oriented. KOH etching is a very simple and cheap technique that allows the fabrication of very interesting structures due to the selectivity of the etch on ⟨111⟩ directions (it stops on {111} planes).[21,22] In Fig. 1 a sketch of a silicon wire fabricated with this technique is represented. The wire is ⟨110⟩ oriented and the transverse section is an isosceles trapezoid, where sloping sides are {111} planes; the angle $\alpha$ is 35.3° ($\tan(\alpha)=1/\sqrt{2}$) and at the base $\beta$ is 54.7. The width $w$ of the top base is defined by the lithography while the width $W$ of the bottom base is determined, once fixed $w$, by the thickness $t$ of the silicon top layer: $W=w+2t/\sqrt{2}$.

The main advantage of this technique is that a trapezoidal cross section allows an easy reduction of the wire dimensions by successive oxidation steps. The oxide growth proceeds not only from the top, but also from the sloping sides of the section, as schematically reported in Fig. 2. If the minor base and the thickness are correctly designed, a trian-

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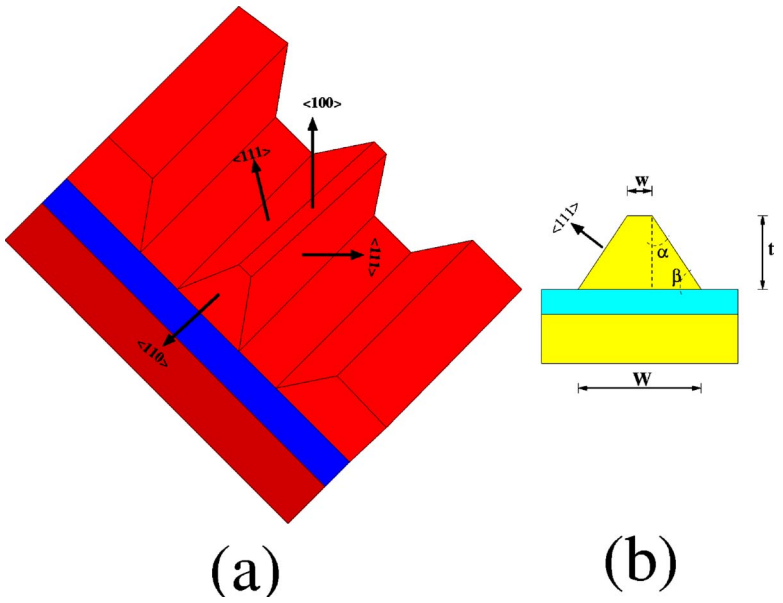



FIG. 1. Perspective (a) and cross section (b) views of the proposed structure fabricated on a SIMOX wafer.

gular silicon cross section is formed after a suitable oxidation time. Once the triangular section has been obtained, oxidation further reduces the wire dimensions preserving the section shape. In this way lithography can be relaxed because, even if the initial $w$ is not very small, a strong reduction of the device section can be performed. A relationship for a rough estimation of $w$ and $t$ can be obtained by elementary trigonometry with the hypothesis of uniform silicon dioxide growth rate, and it is $w < 2t \tan(\beta/2)$. However, this is a very simplified relationship because the oxide growth rate in the $\langle 111 \rangle$ direction of the sloping walls is different from that in the $\langle 100 \rangle$ direction of the section top (surface of the wafer): at the beginning, in the reaction controlled regime, the oxidation rate ratio between the two directions is about 1.7,[23] and this helps the formation of the triangular shape; afterward, in the diffusion controlled regime, rates become comparable. Moreover, the simplified relationship $w < 2t \tan(\beta/2)$ does not consider oxidation from the bottom of the section due to oxygen diffusion through the buried $SiO_2$ layer. A precise evaluation of the oxide growth and a correct design of $w$ and $t$ can be obtained by using numerical methods. Simulations of dry oxidation processes at 1000 °C have been performed using ATHENA (Ref. 24) software. Figure 3 shows simulation results for a trapezoidal section wire with $w=70$ nm and $t=110$ nm. A triangular section is obtained with an oxidation time of 60 min, and then the reduction proceeds, giving very small one-dimensional (1D) structures before the full oxidation of the section, obtained after 180 min. In Fig. 4 the oxidation process of a trapezoidal section with $w > 2t \tan(\beta/2)$ ($w=240$ nm and $t=110$ nm) is shown: in this case a triangular section is not formed and only a bidimensional structure can be fabricated. Simulations show that even for very long times the section is not completely oxidized, probably due to mechanical stress in the silicon core that reduces the oxidation rate. Figure 5 shows oxidation processes of a rectangular section, like the one produced by lithography and directional dry etching, with $w < 2t$; as in the case of Fig. 4, only bidimensional structures can be fabricated. If the ratio $t/w$ is sufficiently high, oxidation is faster in the middle and two almost monodimensional structures remain in the top and bottom of the section.[16]

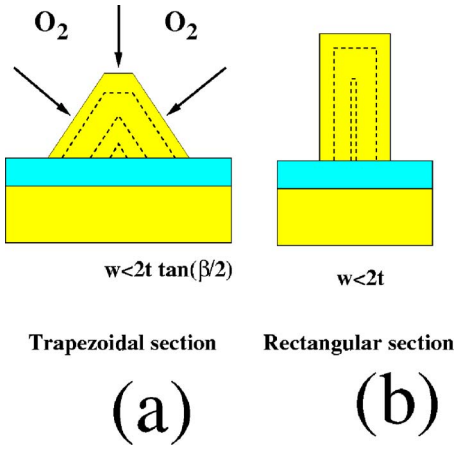



FIG. 2. Schematic view of the oxidation of a silicon wire with trapezoidal (a) and rectangular (b) cross sections.

Another advantage of defining wires by means of a wet anisotropic etching is that the etch follows exactly well defined crystalline planes. This means that possible roughness or imprecisions of the mask edge are smoothed during the silicon etch process itself. Therefore the fabrication of uniform wires with high longitudinal to transverse dimension ratio is made easier. Wires with a regular transverse shape of a few tens of nanometers can be obtained even for length in the micrometer range.

The oxide grown for the section reduction can also be used as an insulator layer for a metal (or polysilicon) gate. Therefore the conduction channel can be further squeezed in all directions by the action of both top gate and substrate acting as a back gate, as schematically shown in Fig. 6.

## III. SILICON NANOWIRE FABRICATION

Two different mask layouts, schematically shown in Fig. 7, have been experimented in order to fabricate silicon nano-

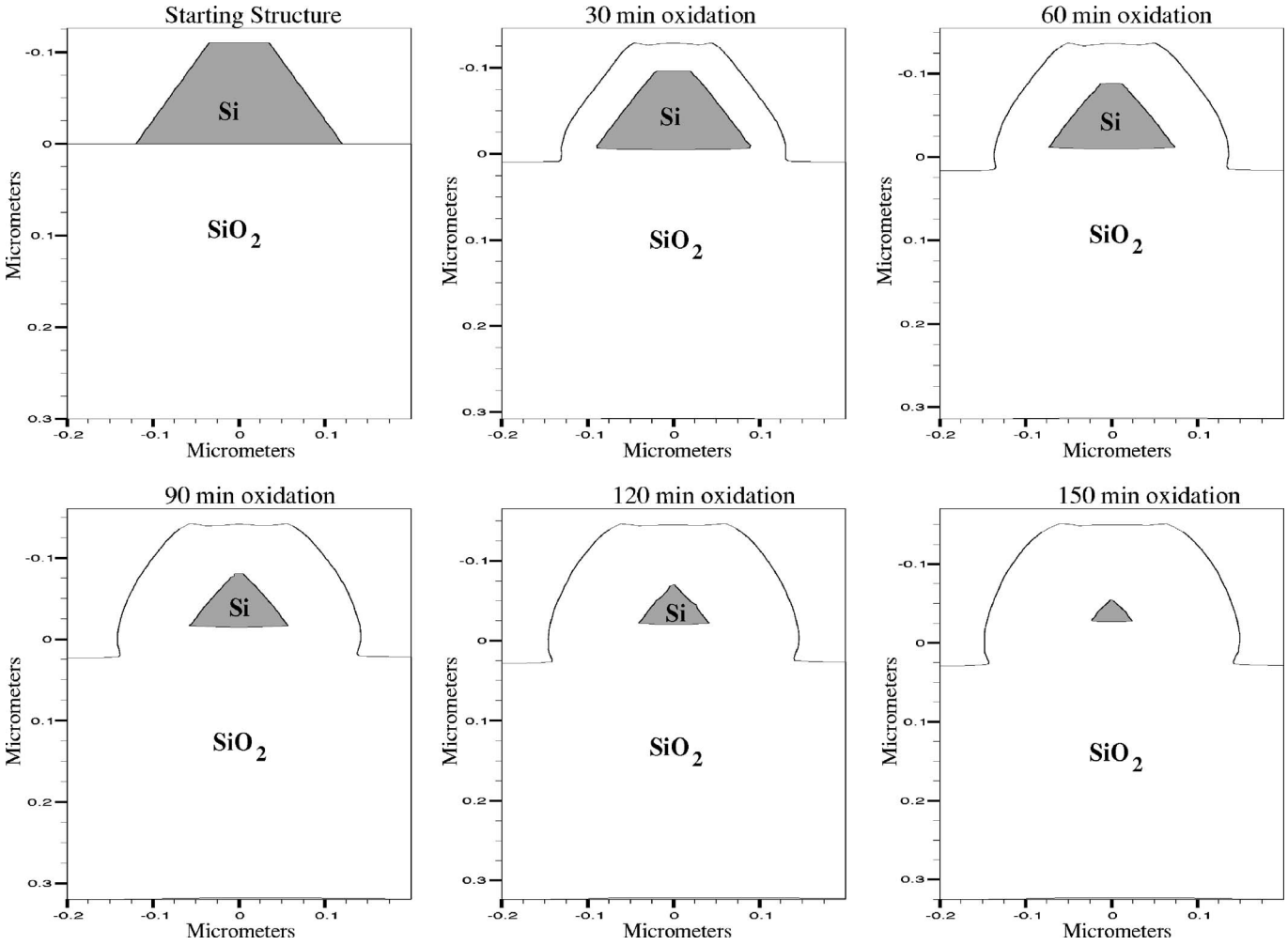



FIG. 3. ATHENA (SSUPREM) oxidation simulation of a trapezoidal section, with $w=70$ nm and $t=110$ nm. After 60 min the silicon core is triangular, and the section is completely oxidized after 180 min of processing.

wire with triangular section. The type-*A* layout has already been employed in a previous work,[25] and here it is reported for comparison with the type-*B* layout. The starting material is a commercial silicon implanted oxide (SIMOX) wafer ⟨100⟩ oriented and *p* doped (resistivity 10 Ω cm). The wafer has a 190 nm thick silicon layer insulated from the substrate by a buried silicon dioxide layer of 380 nm. A sacrificial silicon dioxide top layer is grown and removed by buffered HF (BHF) for reducing the top silicon layer thickness to 150 nm. An 80 nm thick silicon dioxide layer has then been regrown by thermal dry oxidation and patterned by means of electron beam lithography; this layer acts as a mask for the successive KOH etch. A two layer polymethylmethacrylate (PMMA) based high resolution process is used (996 K 3% in anisole on 350 K 3% in anisole, both layers spun at 4000 rpm, baked on a hot plate for 1 h at 200 °C). Both mask layouts are line based patterns (see Fig. 7). Each structure is made of two parts written in the same lithographic step: one written with high resolution (acceleration voltage of 30 kV, single passage with a writing step of 2.5 nm, and line dose about 25 nC/m), and the other written at low resolution (acceleration voltage of 30 kV, single passage with a writing step of 25 nm, and line dose about 50 nC/m). The low resolution part provides lines for insulation trenches around each device and its conduction pads. Alignment markers (not shown in the figure) for successive lithographic steps are also provided. After exposure, the resist is developed for 30 s in isopropyl alcohol (IPA): methyl-isobutyl ketone (MiBK) (3:1), rinsed in IPA, and blow dried with pure nitrogen.

The patterned PMMA is used as a mask for the successive $SiO_2$ etch with BHF solution, performed at room temperature and calibrated for etching 80 nm+/−2 nm. After PMMA stripping, the KOH anisotropic etching is then performed, using a solution 35% in weight, saturated with isopropyl alcohol, at 45 °C. The IPA saturation gives cleaner surfaces and reduces the etch rate.[26,27]

In Fig. 7 the two high resolution patterns are reported. The first one (type *A*) exploits the underetch of the $SiO_2$ mask, aligned to the ⟨110⟩ directions. The two tilted lines are perpendicular to ⟨100⟩ directions in such a way that the etch proceeds very fast under the $SiO_2$ mask, but it is stopped on {111} planes in the middle region where the triangular wire is formed. Its transverse section (minor base width *w*) is determined by the initial distance of the two horizontal lines, as shown in the sketch of Fig. 8, and proximity effects do not play an important role due to the distance of the lines. The wire length is determined by the etching time whose maxi-

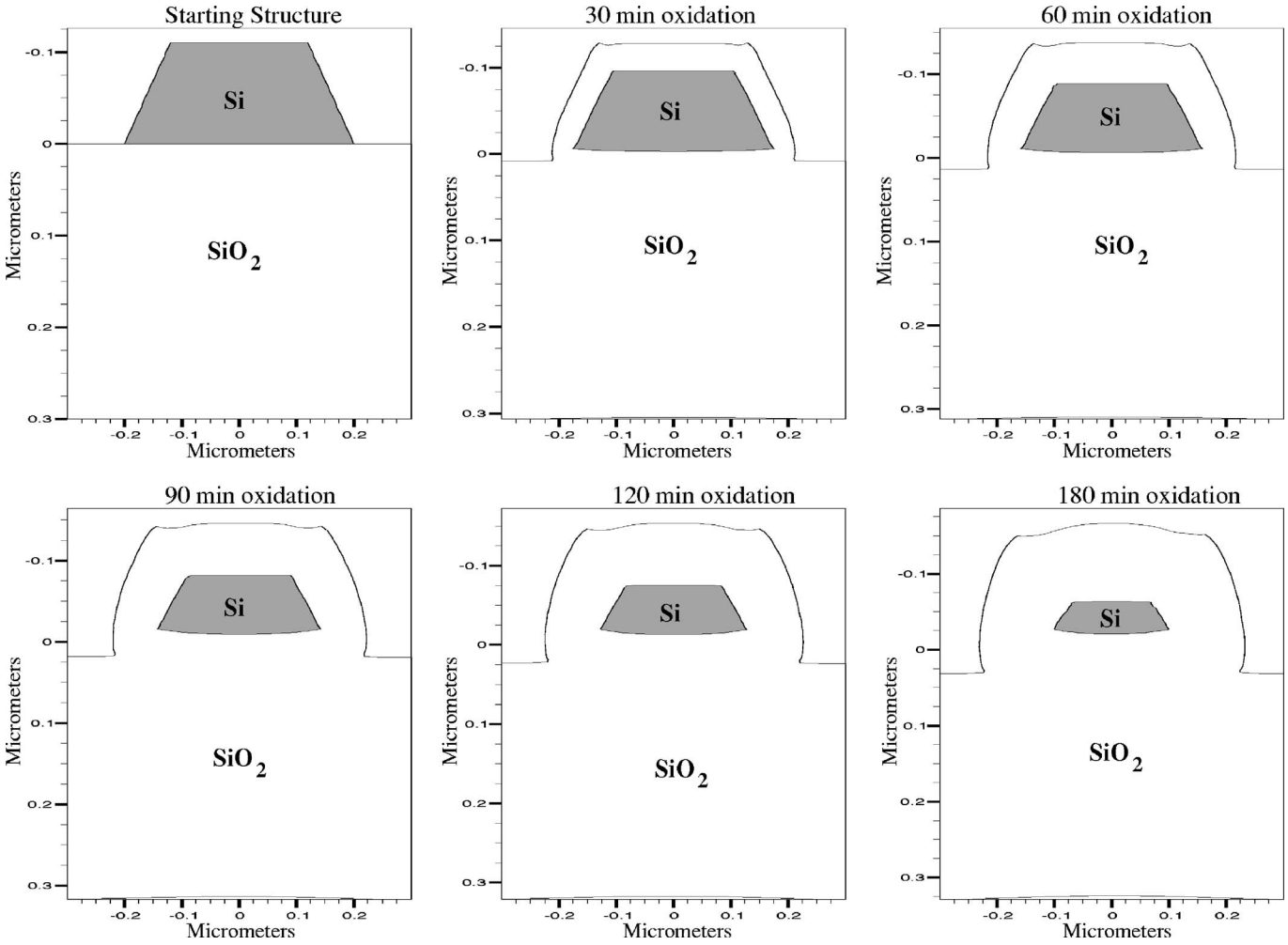



FIG. 4. ATHENA (SSUPREM) oxidation simulation of a trapezoidal section, with $w=240$ nm and $t=110$ nm $[w>2t\tan(\beta/2)]$. The silicon core never reaches a triangular shape and even with very long times, it is not possible to obtain a full oxidation.

mum value is limited by the transverse dimensions that are reduced with the very low etch rate of the ⟨111⟩ planes. In principle, the value of the longitudinal to transverse dimension ratio can be equal to that of the etch rate ratio between the ⟨100⟩ and ⟨111⟩ directions. For fabricating short wires a correct calibration of the etch time is required. In Fig. 8 a sketch of the underetch is shown. The scanning electron microscopy (SEM) images show the $SiO_2$ mask patterned (type-*A* mask of Fig. 7) and the silicon wire formed under the mask by the KOH etch; in the inset an enlargement of the central region of the wire is shown. By using the type-*B* mask both the minor base width *w* of the transverse section and the length of the wire are determined by the electron beam lithography. The KOH etch time is not critical, but it must only be sufficiently long for removing the silicon top layer (the length of the wire is determined by the mask layout). Irregularities in the mask are reduced by the selectivity of the etch that follows the ⟨111⟩ planes, and even very long wires show a uniform transverse section. It is also easy to fabricate very short wires: the longitudinal dimension of the wire is limited only by the resolution of the electron beam lithography. The transverse dimensions of the wire are determined by the distance of the two lines, and are strongly affected by the proximity effect. For this reason, different from the case of the type A mask, the writing dose must be carefully calibrated. In Fig. 9 a SEM image of the structure obtained after KOH etch, and before the $SiO_2$ mask strip, is shown. The wire is 3 $\mu$m long and, despite the fact that the mask is not very regular along the structure, the minor base width *w* is 70 nm for all the lengths of the wire: in the inset an enlargement, showing the silicon wire under the irregular $SiO_2$ mask, is reported.

After KOH processing, the oxide mask is stripped by BHF etch, which also acts on the buried oxide in the areas where silicon has been removed. By making the etch time long enough it is also possible to suspend the silicon wire, and the successive oxidation step could produce an even stronger reduction acting on all the sides of the wire. However, the suspension of the wire has been avoided because it would be very difficult to contact the gate on the top of a suspended wire. The transverse section reduction is performed by dry oxidation at 1000 °C. In this step the uniformity of the section along the wire is essential to avoiding the formation of multiple silicon isles divided by $SiO_2$. Figure 10 shows SEM images of the silicon wire before (a) and after (b) reduction by oxidation. Fig. 10(a) shows the wire before oxidation: the top base is 70 nm and the bottom base is 230 nm, compatible with a thickness of the top silicon layer

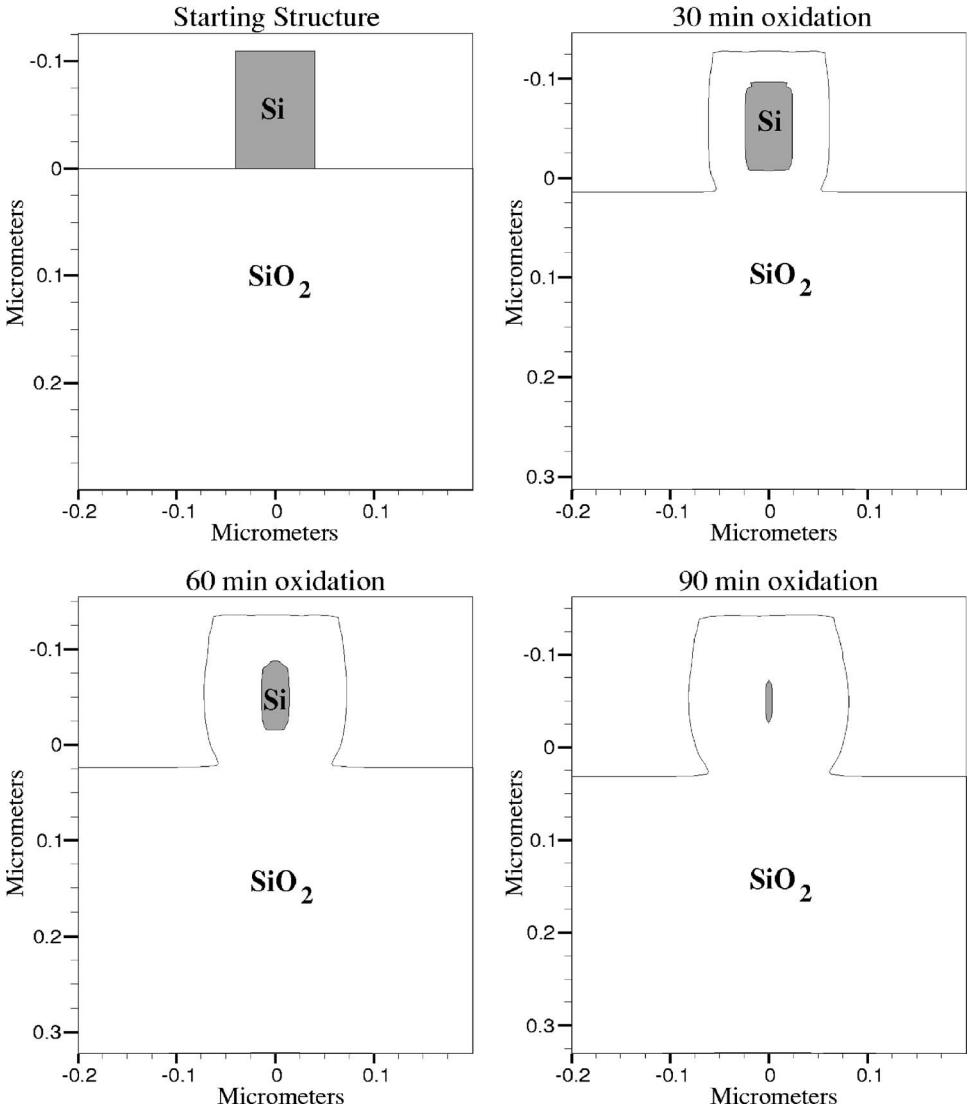



FIG. 5. ATHENA (SSUPREM) oxidation simulation of a rectangular section, with $w=80$ nm and $t=110$ nm.

of 110 nm. The photo in Fig. 10(b) has been taken after dry oxidation for 120 min at 1000 °C and oxide removal by BHF etch. The sample is tilted at 30° and rotated to make the triangular shape more evident. Figure 11 shows an ATHENA simulation of an oxidation process for a trapezoidal section with dimensions shown in Fig. 10(a): the dimensions of the final triangular section are comparable with those of Fig. 10(b). At this point a second lithographic step is required for metal pad definition. A double layer PMMA process is as follows: $996\times10^3$ molecular weight (MW) 6% in anisole on $350\times10^3$ MW 6% in anisole, both spun at 5000 rmp and baked for 1 h at 200 °C on a hot plate. Pad areas of 150 $\times 150$ $\mu$m$^2$ are written and aligned to the insulation trenches previously obtained. The alignment step has been performed on rectangular markers, obtained with the previous KOH step as holes in the silicon top layer: a deconvolution algorithm for negative marker detection by electron beam has been designed and successfully tested. After resist development in IPA:MIBK 1:1 for 30 s, BHF etch is used to clean the pad areas from silicon dioxide (oxide windows). Before resist strip, an 80 nm aluminium layer is then deposited by thermal evaporation, and lift-off in hot acetone is performed for pad definition; in this way pads became self aligned with oxide windows. A third lithographic step is then performed for top gate definition. This process step is similar to the previous one, apart from the window opening by BHF etch before aluminium evaporation: in this way the oxide layer grown for device reduction is also used as a gate oxide.

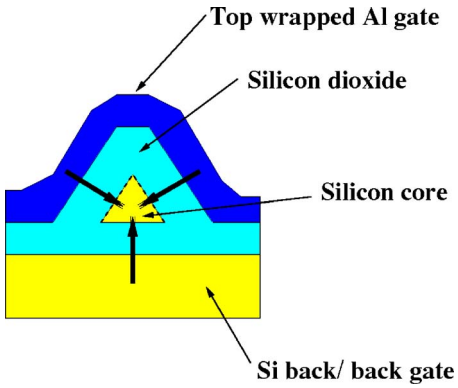



FIG. 6. A sketch of a triangular section of the silicon wire. A gate on top of the $SiO_2$ layer has been deposited. Both the top aluminium gate and the bottom (back) silicon gate act on the triangular silicon core.

Silicon wires with source and drain contacts, and a gate on top of the wire, or better on the sloping walls around the

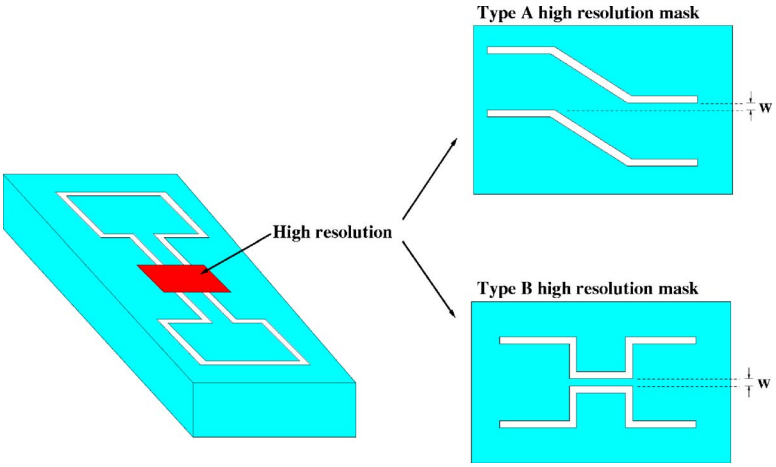
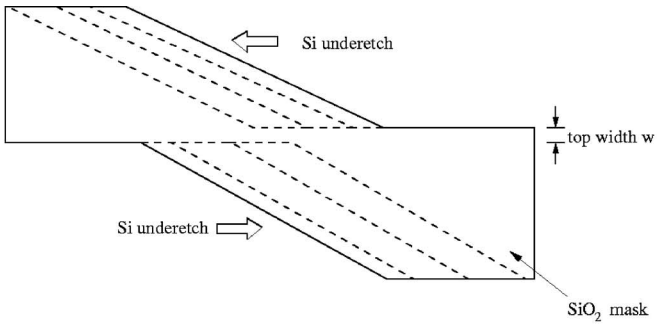



FIG. 7. A sketch of the patterns. Left: the pattern for the insulation trenches that define the pad contacts; Right: the two high resolution patterns used for wire definition.

wire, have been obtained by means of this technique. The bottom silicon layer can act as a second control gate. Several devices are realized on the same chip, which is then mounted on a TO8 package by silver conductive paste, to provide a contact to the bottom silicon layer. Alluminium pads (sources, drains, and top gates) are then connected to the package pins by wedge bonding.

## IV. CHARACTERIZATION OF TRIANGULAR SILICON NANOWIRES

In order to determine the potential distribution induced by the gate bias in a wire with triangular cross section,[28] semiclassical electrostatic simulations have been performed by means of ATLAS (Ref. 29) simulator. Low and high doped



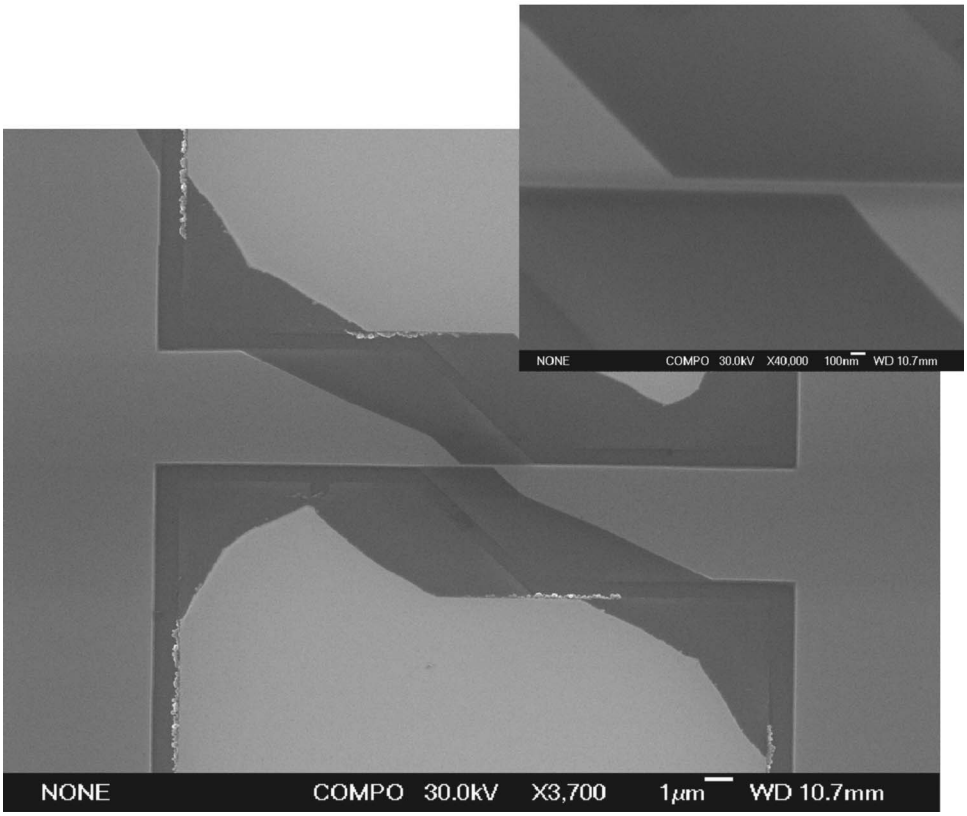




FIG. 8. SEM images of a silicon wire obtained with the mask A. In the inset an enlargement of the central area of the wire is shown. In the sketch the proceeding of the silicon etch under the $SiO_2$ mask is reported.

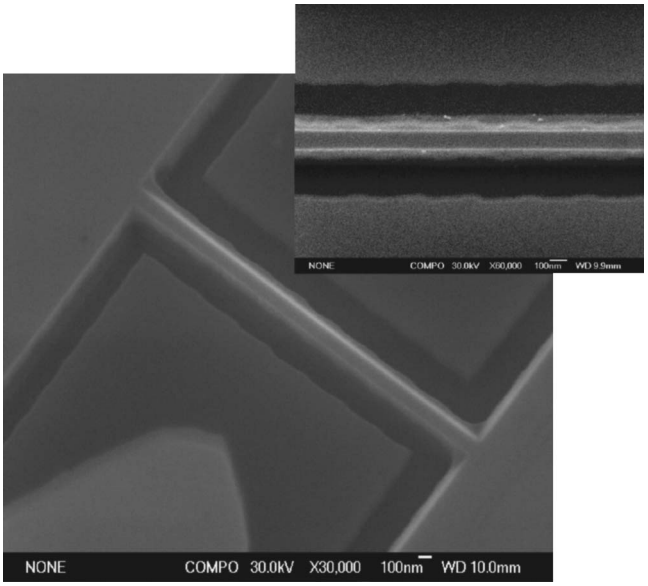



FIG. 9. Images of a silicon wire obtained with mask B. In the inset an enlargement of the wire, showing the quite irregular $SiO_2$ mask and the silicon wire underneat, is shown.

wires have been simulated obtaining hole and electron concentrations in the section. Figure 12 shows the solution for a $p$-type wire ($5\times10^{17}$ cm$^{-3}$) obtained by applying a bias of 1.5 V to gates positioned on the top and on the bottom of the section shown in Fig. 11, and $V_{DS}=0$. As expected, biasing effects are stronger on the corners of the triangular section and, consequently, in these areas depletion is stronger; the central conducting region is almost circular and can be restricted in an easy way by using a suitable doping and biasing. With a low doped wire it is possible to fully deplete the section with a very low voltage, and eventually to bring it to inversion. Figure 13 shows the electron concentration as obtained by a simulation of a $p$-type-doped wire ($2\times10^{15}$ cm$^{-3}$), with an applied bias of 50 and 0.8 V to the top and bottom gates, respectively. The wire becomes fully depleted by holes and is in inversion condition. Electron accumulation is stronger in the corners of the silicon cross section where the electrical field is higher. Electrical behavior in silicon nanowires ($p$ doped $2\times10^{15}$ cm$^{-3}$), fabricated with the same process used for the structure reported in Fig. 10, has been investigated. As far as the wire dimensions are concerned, SEM imaging has allowed a measurement of the length, while the section is covered by oxide and only an estimation of the dimensions is possible. Roughly a 10% variation of cross-section dimensions with respect to those of the structure of Fig. 10 has been estimated in different runs. A HP4145B parameter analyzer has been used to measure the current through the wire as a function of top gate and back gate biasing. The two contact pads (conventionally called source and drain) of $150\times150$ $\mu$m$^2$ have been used

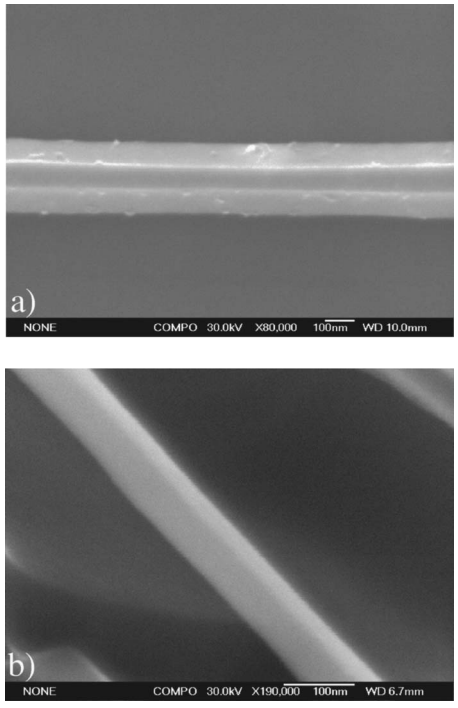



FIG. 10. Top view of a silicon wire after KOH etch and $SiO_2$ mask strip (a). It shows the top base and the sloping walls which are ⟨111⟩ planes. The same wire in a after oxidation (120 min at 1000 °C) and $SiO_2$ removal by BHF etch. (b) The sample is tilted and rotated for making the triangular shape more evident.

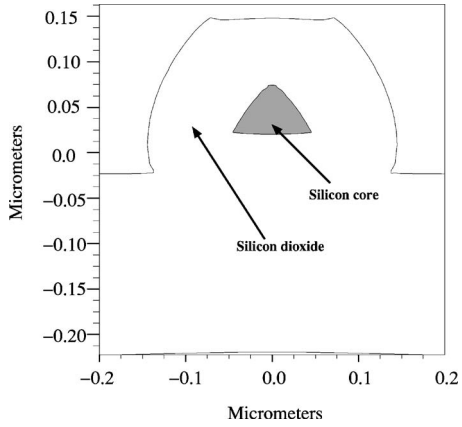



FIG. 11. ATHENA (SSUPREM) oxidation simulation of trapezoidal section, with $w=70$ nm and $t=110$ nm, and oxidation time of 120 min at 1000 °C.

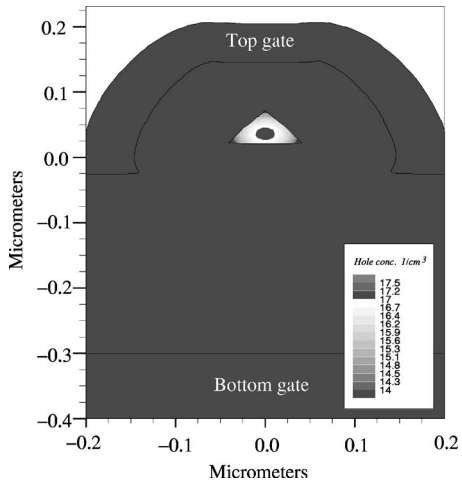



FIG. 12. Hole concentration of a wire cross section, $p$ doped $2\times10^{17}$ cm$^{-3}$, with a bias of 1.5 V applied to both gates (ATLAS simulation). The structure is partially depleted, and a conductive region with high hole concentration is left in the middle of the section.

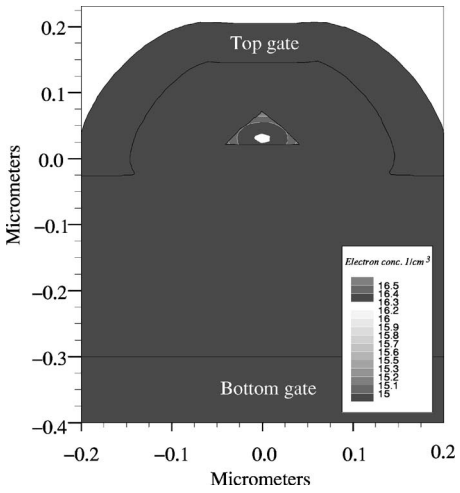



FIG. 13. Electron concentration in a wire cross section, $p$ doped $2\times10^{15}$ cm$^{-3}$, with a bias of 0.5 and 0.8 V applied on the top and bottom gates, respectively (ATLAS simulation). The structure is in inversion, and electron accumulation is stronger in the corners of the triangular section.

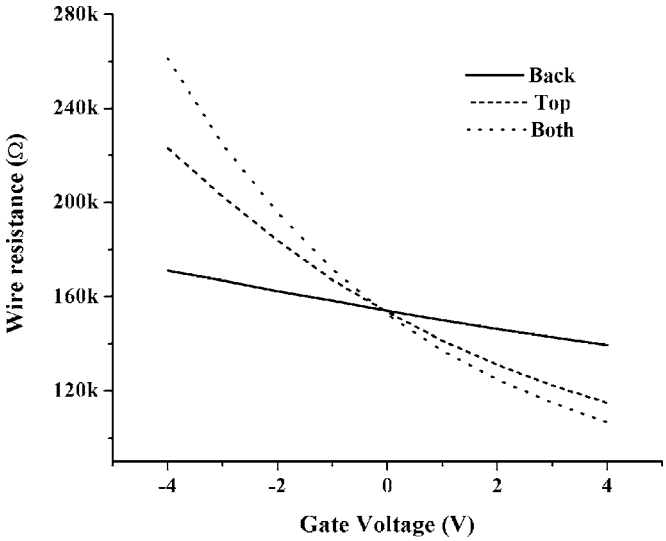



FIG. 15. Wire resistance as a function of gate bias voltage. The three curves are related to the bottom gate, top gate, and both gate biasing.

for a longitudinal bias of the wire and for current measurement. We should point out that even if the pad areas are not heavily doped, their surfaces are very large and Schottky barriers on the contacts became ineffective on the conduction behavior. Figure 14 shows $I_{DS}/V_{DS}$ characteristics taken for different values of back gate voltage $V_{GbottomS}$ ($V_{GtopS}=0$), for a 1.2 $\mu$m long wire. At room temperature $I_{DS}/V_{DS}$ characteristics show a linear symmetric behavior for $V_{DS}$ voltages in the range $(-1,1)$ V. In the inset, the wire resistance, calculated by a linear fit of each $I$-$V$ characteristic, is reported as a function of gate voltage. The monotonic decreasing of the resistance, with respect to the increasing of the bias voltage, is consistent with the fact that the wire is in inversion and conduction is driven by electrons: this confirms the simulation results. A fit with an exponential decay function is also reported; this shows that the electron concentration varies exponentially with the gate bias. For all the investigated wires the resistance increases for negative bias; this can be explained, making the hypothesis that the wire depletion is very strong due to both the difference between metal and silicon work functions and oxide charges.

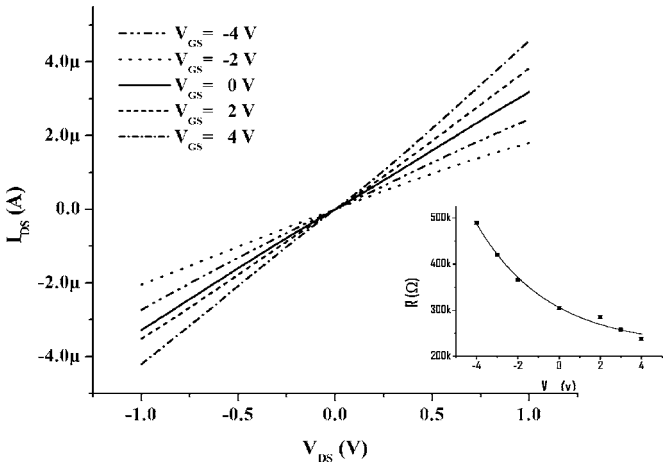



FIG. 14. Characteristics for different values of back gate voltage (top gate connected to the source).

The effect of the top gate biasing, bottom gate biasing, and simultaneous biasing of both gates has been studied. Figure 15 reports the resistance of a 0.6 $\mu$m long wire as a function of gate voltage. It is evident that the resistance variation is stronger by using the top gate voltage with respect to the bottom gate voltage, because both the top gate is insulated by a thinner $SiO_2$ layer and the top gate acts on two sides of the device. The effect of the bias is maximized, short circuiting the two gates together, as reported in the third curve of Fig. 15.

$I$-$V$ characteristics have been measured at low temperatures. The TO8 case has been mounted on an open circuit cryostat, supplied with liquid nitrogen, and a heater has been used for temperature control. Figure 16 shows $I_{DS}/V_{DS}$ characteristics taken at low temperatures with both gates connected to the source ($V_{GS}=0$). For temperatures below 200 K the gate biasing of the device became very difficult because the wire resistance changed very slowly for a change of the

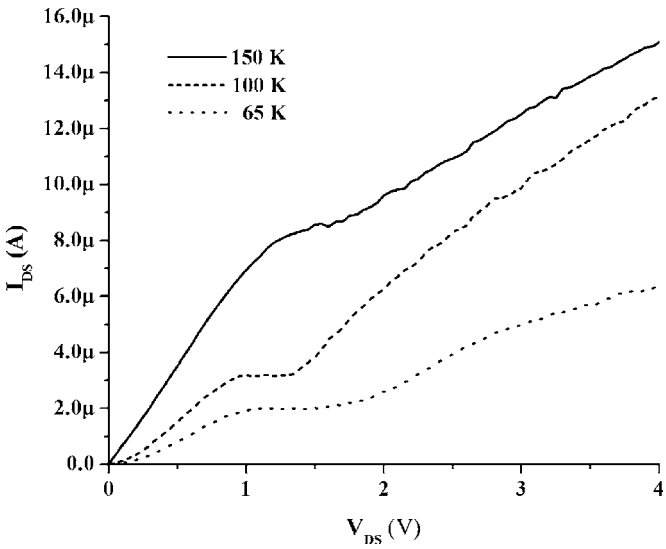



FIG. 16. $I_{DS}/V_{DS}$ characteristics taken at 150, 100, and 65 K, for a zero bias applied to both gates.

gate voltage. This confirms that the conduction in the wire is driven by electrons in inversion layers; generation time in an inversion layer increases exponentially with decreasing temperature. For this reason we preferred to perform temperature measurements at a fixed gate bias of 0 V. It should be noted that the wire is in inversion condition for different gate voltage values, as reported in Fig. 14. The characteristics are not linear any more, and increasing the $V_{DS}$ a plateau at about 1 V is clear and well defined at 65 K and the plateau is still visible for temperatures up to 150 K. A possible hypothesis is that this effect is related to 1D effects due to the electron accumulation at the corners of the silicon triangular section.

In order to confirm the 1D hypothesis, gate bias effects at low temperatures should be investigated. This will require both an accurate study of generation times in the inversion state and a high doping of the contact areas which are used as electron reservoir. Moreover, for a complete comprehension of these phenomena, the wire electrical behavior should be investigated as a function of the silicon doping.

## V. CONCLUSIONS

Fabrication processes for silicon nanowire with triangular section, based on SIMOX substrate, electron beam lithography, and silicon anisotropic etching, are described. Simulations of an oxidation process applied to a trapezoidal section show that it is possible to reduce the device cross section in a significant way. Processes allow the deposition of a gate that, with the silicon substrate acting as a back gate, wraps the device all around.

Electrical simulation confirmed that the field is stronger on the corners of triangular section and that low doped wires can be easily driven in inversion state with an accumulation of carriers at the corners of the section. Measurements on low doped wires showed that they are in inversion state, even for negative values of bias voltage; this is probably due both to the difference between the metal and silicon work functions and to oxide charges. Low temperature measurements showed a plateau in the $I/V$ characteristic of the silicon wires for temperatures below 150 K.

Electrical characterization of structures with doped contacts and with different silicon doping levels is required in order to reach a full comprehension of the phenomena involved in the conduction of the wires.

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