Aging Benefits in Nanometer CMOS Designs

Daniele Rossi, *Member, IEEE,* Vasileios Tenentes, *Member, IEEE,* Sheng Yang, Saqib Khursheed, Bashir M. Al-Hashimi *Fellow, IEEE*

***Abstract*—In this paper, we show that BTI aging of MOS transistors, together with its detrimental effect for circuit performance and lifetime, presents considerable benefits for static power consumption due to sub-threshold leakage current reduction. Indeed, static power reduces considerably, making CMOS circuits more energy efficient over time. Static power reduction depends on transistor stress ratio and operating temperature. We propose a simulation flow allowing us to properly evaluate the BTI aging of complex circuits in order to estimate BTI-induced power reduction accurately. Through HSPICE simulations, we show 50% static power reduction after only 1 month of operation, which exceeds 78% in 10 years. BTI aging benefits for power consumption are also proven with experimental measurements.**

***Index Terms*—BTI aging, leakage current, static power, nanometer technology, energy-efficiency**

I. Introduction

Reliability of aggressively scaled electronic systems is one of the most critical concerns of designers. It is being increasingly challenging to design systems that will provide users with the intended service over time. Particularly, scaling to 32nm technology nodes and below leads to reliability effects that are characterized by a progressive degradation of the performance of devices and system components induced by aging phenomena [1]. Bias temperature instability (BTI), hot carrier injection (HCI) and time dependent dielectric breakdown (TDDB) are the main aging mechanisms experienced by aggressively scaled devices [2]. Negative BTI observed in pMOS transistor is the dominant one in the latest process technology [2], and is unanimously recognized as one of the primary parametric failure mechanisms for modern ICs [2]–[4]. However, with the use of high-K dielectric stacks, also positive BTI (PBTI) exhibited by nMOS transistors is significant and can no longer be neglected [5]. BTI manifests with an increase over time in threshold voltage value (V_{th}) of MOS transistors, mainly due to the creation of positively charged interface traps, when transistors are biased in strong inversion [6]. The main BTI aging effect usually discussed in the literature is the propagation delay increase over time induced by V_{th} degradation. If this performance degradation exceeds circuit time margins, it may lead to circuit failure and reduce lifetime of electronic systems [2], [3], [7].

Differently from most of the research results related to BTI aging, which focus only on its detrimental effects, in [8], [9] we have highlighted that logic and memories implementing low-power techniques are benefited by BTI aging. Particularly, we showed that leakage power reduces in circuits employing power gating and dynamic voltage scaling (DVS) due to BTI aging affecting power switches, making these techniques more efficient over time.

In this paper, we prove that also high performance nanometer CMOS designs are benefited by BTI aging. We show that BTI induces a considerable reduction of static power due to leakage sub-threshold current, making CMOS logic more energy-efficient over time. This reduction depends on operating conditions (stress time and aging temperature). By HSPICE simulations performed considering a simple case study consisting of 10 FO4 cascaded inverters implemented with a 32nm Metal Gate, High-K CMOS technology [10] and different aging temperatures, we show that static power may reduce by more than 50% during the first month of operation, and by more than 75% over 10 years. We then propose a simulation flow for evaluating static power consumption trend over time in complex circuits, accounting for the proper BTI aging degradation. The results obtained for several benchmarks from the IWLS05 benchmark suite confirm those described above, with an average static power reduction ranging from 52.15% after one month of operation to 78.17% after 10 years. This beneficial effect is expected to escalate for more scaled technologies, because of the increase in sub-threshold current [11] and impact of BTI aging [12]. Static power decrease over time due to BTI aging has been also proven with an accelerated aging experiment, using a test-chip manufactured with a 65nm technology. Leakage current reduction up to 11.4% after 526 hours of operation has been measured.

The rest of the paper is organized as follows. Section II introduces the basics of BTI aging. In Section III, through HSPICE simulations, we assess the BTI aging beneficial effects for static power consumption of nanometer CMOS circuits considering a simple case study. In Section IV, we first describe the proposed simulation flow and assess BTI aging benefits for several benchmark circuits. Then, we provide experimental evidence of the BTI aging benefits. Finally, in Section V, we draw some conclusions.

II. Background

Bias temperature instability (BTI) causes a threshold voltage increase of MOS transistors, when they are ON (stress phase) [6]. BTI-induced degradation is partially recovered when MOS transistors are polarized in their OFF state (recovery phase). As per the reaction-diffusion model in [6], BTI originates from the creation of charges trapped at the Si-dielectric interface during the stress phase. The traps generated at the Si-dielectric interface shield the applied gate voltage, thus resulting in a

D. Rossi, V. Tenentes and B. M. Al-Hashimi are with the Department of Electronics and Computer Science (ECS), University of Southampton, UK. E-mail: {D.Rossi, V.Tenentes, bmah}@ecs.soton.ac.uk

S. Yang is with ARM,Cambridge, UK. Email: sheng.yang@arm.com

S. Khursheed is with the Department of Electrical Engineering & Electronics, University of Liverpool, UK. Email: S.Khursheed@liverpool.ac.uk

Manuscript received xxx; revised xxx.

threshold voltage increase. During the recovery phase, the generated traps are partially annealed [6]. Negative BTI (NBTI) is observed in pMOS transistors, and it dominates over the positive BTI (PBTI) observed in nMOS transistors [5], [6].

An analytical model is presented in [5], [13] that allows designers to estimate long term threshold voltage shift. It is:

$$\Delta V_{th} = \chi K \sqrt{C_{ox}(V_{dd} - V_{th})} e^{-\frac{E_a}{kT}} (\alpha t)^{1/6} \quad (1)$$

The parameter C_{ox} is the oxide capacitance, t is the operating time, α is the fraction of the operating time during which a MOS transistor is under a stress condition, k is the Boltzmann constant, T the device temperature and E_a is a fitting parameter ($E_a \simeq 0.08$ [5]). The parameter K lumps technology specific and environmental parameters, and has been estimated to be $K \simeq 2.7V^{1/2}F^{-1/2}s^{-1/6}$ by fitting the model with the experimental results reported in [14]. The coefficient χ allows us to take into account the fact that NBTI ($\chi = 1$) prevails over PBTI ($\chi = 0.5$) [5].

III. BTI Aging Benefits Analysis

We analyze the beneficial effects of BTI aging on power consumption of nanometer CMOS circuits. As known, the total power consumption of a CMOS circuit can be expressed as the sum of dynamic power P_{dyn} and static power P_{st}. Dynamic power is consumed during switching and its value is therefore frequency dependent. It consists of two components: the power required to charge the circuit capacitances (referred to as *switching power*, P_{sw}), and that consumed due to short circuit current flowing from V_{dd} to ground during switching (referred to as *short-circuit power*, P_{sc}) . As for the static power, it is consumed when the circuit is not switching and is due to the leakage current flowing from V_{dd} to ground. It is:

$$\begin{aligned} P_{tot} &= P_{sw} + P_{sc} + P_{st} = \\ &= (C_{eff}V_{dd}^2 + V_{dd}I_{sc}\tau_{sc})f_{ck} + V_{dd}I_{leak}, \end{aligned} \quad (2)$$

where C_{eff} is the effective capacitance accounting for the actual switching activity of the circuit, I_{sc} is the average short circuit current flowing from V_{dd} to ground during switching for an interval time equal to τ_{sc}.

A. Simulation Set-up

We consider here a simple case of 10 cascaded inverter implemented with a 32nm Metal Gate, High-K CMOS technology [10], with a supply voltage $V_{dd} = 1V$. We assess the trend over time of the threshold voltage increase ΔV_{th}, as well as of the consequent aging benefits on power consumption for different aging temperatures $T_A = 25^oC, 50^oC$ and 75^oC, and constant stress ratio $\alpha = 0.5$. In Figure 1, we show the approach followed to embed aging effects in our simulation flow. Following the procedure in [14], [15], given power supply V_{dd} and operating conditions (aging temperature T_A and stress ratio α), the ΔV_{th} degradation is estimated. The ΔV_{th} value obtained for each considered operating time interval is then utilized to customize the HSPICE device model and simulate the circuits with the proper BTI degradation. Since leakage current exhibited by a gate depends on input configurations, we average the values obtained for the two different input values, considering them as equally likely.

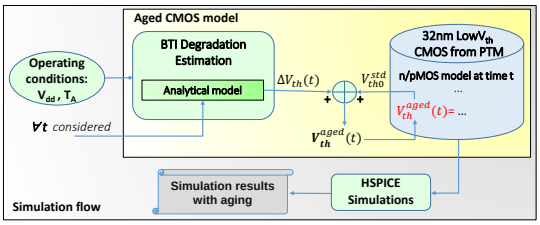


Fig. 1. Simulation flow with embedded aging effects.

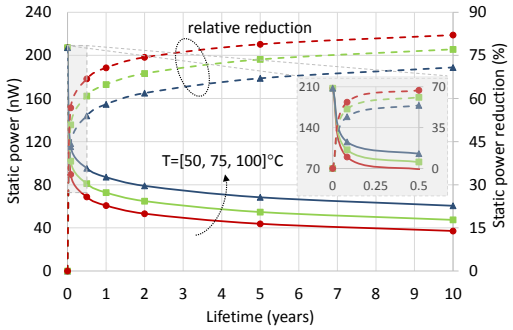


Fig. 2. Trend over time of the static power for different temperatures (solid lines) and relative reduction over the static power at t=0.

B. BTI Aging Effects on Static Power

In CMOS designs, static power consumption P_{st} is due to leakage current flowing from V_{dd} to ground when a circuit is idle. Leakage current has two main contributors [16]: sub-threshold current and gate current. Sub-threshold current contribution dominates, since gate current can be well controlled by the use of high-k dielectrics. It is $P_{st} = V_{dd}I_{leak}$, which can be expressed as [16]:

$$P_{st} \simeq V_{dd}\mu C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 e^{\frac{q(V_{gs}-V_{th})}{nkT}}\left(1 - e^{\frac{-qV_{ds}}{kT}}\right), \quad (3)$$

where C_{ox} is the dielectric capacitance, W and L are the MOS transistor channel width and length, respectively, q is the electron charge, k the Boltzmann constant, T the temperature, and n a parameter that depends on device fabrication.

Since the main BTI effect is to increase V_{th}, as shown in (1), we expect that static power decreases over time. This is confirmed by the obtained HSPICE simulation results shown in Figure 2, which depicts the trend over time of P_{st} for the considered NOT chain. As we can see, after only 1 month of operation, P_{st} reduction is well above 40% for all the three considered aging temperature, exceeding 60% for $T_A = 100^oC$. It further increases up to 58%-71% after 1 year and, after 10 years of operation, P_{st} reduction is in the range 70%-81% for the considered operating conditions.

C. BTI Aging Effects on Dynamic Power

As previously discussed and highlighted in (2), dynamic power comprises of two contributions: the switching power P_{sw} due to the charge of the capacitances of circuit nodes; the short-circuit power P_{sc} accounting for the current flowing from V_{dd} to ground during switching. P_{sw} is not affected by aging and dominates over P_{sc}, which represents around 10% of the switching power [16].

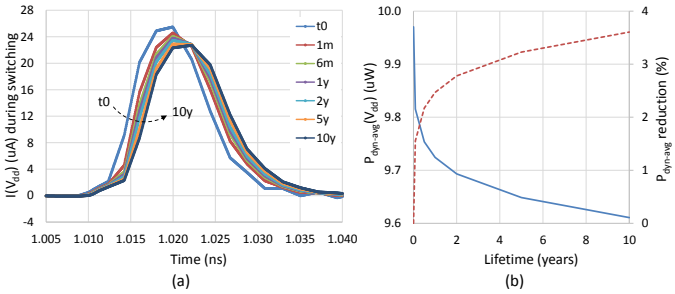


Fig. 3. (a) Dynamic power consumed in a single switch by an inverter for different lifetimes ($T_A = 75^oC$); (b) trend over time of the average dynamic power (solid line) and relative reduction over the power at t=0 (dashed line).

In turn, P_{sc} varies with BTI aging. Indeed, it is proportional to the short circuit current I_{sc} flowing from V_{dd} to ground during the time interval τ_{sc}, which depends on the rise/fall time τ. Both I_{sc} and τ_{sc} are affected by BTI aging so as they have an opposite effect on P_{sc}. As for I_{sc}, its maximum value decreases with BTI aging, whereas the time interval τ_{sc} increases as the circuit degrades. According to [17], P_{sc} for a symmetric CMOS gate without load is:

$$P_{sc} \simeq \frac{K_{eq}}{12}(V_{dd} - 2V_{th})^3 \tau f, \tag{4}$$

where K_{eq} is the equivalent conductance of the gate network (either pull-up or pull-down). The term depending on the voltages clearly decreases with BTI aging. In turn, $\tau \simeq 0.8\tau_{sc}$ [17] slightly increases. It is $\tau = R_{eq}C_{out}$, where C_{out} is the load capacitance and $R_{eq} \propto 1/(V_{gs} - V_{th})$ is the equivalent resistance of the switching network. As a result, the P_{sc} is expected to slightly decrease over time. This analysis is confirmed by the simulation results shown in Figure 3. The figure depicts the dynamic power consumed during a 0-to-1 switch focusing on a single NOT gate in the chain (Figure 3(a)), and its trend over time (Figure 3(b)). The variation can be attributed to short circuit power P_{sc}. As can be seen, it slightly decreases as circuit ages, with a 3.7% reduction after 10 years of operation. Since the impact of aging on dynamic power is rather limited, yet beneficial, in the reminder of the paper we focus on the aging benefits on static power only.

IV. Aging Benefits for Complex Circuits

In order to evaluate the aging benefits for complex circuits, the proper BTI aging for all the gates composing the considered circuits must be accounted for. As known, this depends on input values, hence on workload [1]. If the assessment of BTI aging is straightforward for 1-input gates (inverters), as considered in the previous subsection, a more elaborated analysis is required when the number of gate inputs increases.

A. Aging Benefits Evaluation for Basic Gates

As introduced in [18], the stress of each transistor of a 2-input logic gate depends not only on its input voltage (0V or V_{dd}), but also on the status of the other transistors of the logic gate. As an example, consider a 2-input NAND gate and denote by MN1 the nMOS transistor connected to the NAND output, and by MN2 the nMOS transistor connected to ground. When both MN1 and MN2 are ON, it is $V_{GS1} = V_{GS2} = V_{dd}$.

TABLE I
Stress ratio evaluation for 3-in NAND gate

IN1	IN2	IN3	MP1	MP2	MP3	MN1	MN2	MN3
0	0	0	s	s	s	r	r	r
0	0	1	s	s	r	r	r	s
0	1	0	s	r	s	r	x	r
0	1	1	s	r	r	r	s	s
1	0	0	r	s	s	r	r	r
1	0	1	r	s	r	r	r	s
1	1	0	r	r	s	r	r	r
1	1	1	r	r	r	s	s	s
Avg stress ratio			0.5	0.5	0.5	0.125	0.25+x/8	0.5

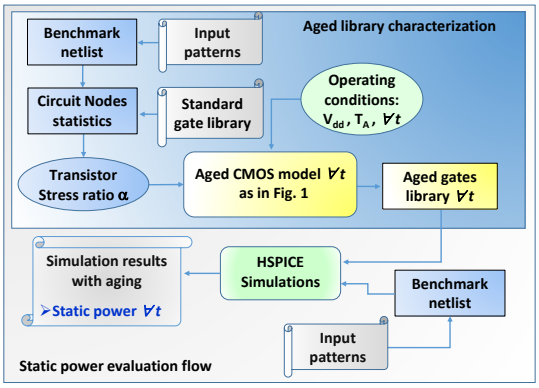


Fig. 4. Proposed flow for static power evaluation.

Therefore, according to (1), they are both under stress. If now MN2 is turned off ($V_{GS2} = 0$), it undergoes a recovery phase. Moreover, since the source of MN1 is charged up to $V_{dd} - V_{th}$, it results $V_{GS1} = V_{th}$. Therefore, according to (1), also transistor MN1 undergoes a recovery phase, although its input is equal to logic 1. This analysis is extended to a 3-input NAND gate, and stress (s) or recovery (r) conditions for each transistor is reported in Table I. The last raw report the average stress ratio values, computed by considering the input patterns as equally likely. Transistor MN1 is connected to the NAND output, whereas MN3 is connected to ground. As can be seen, all parallel pMOS transistors exhibit the same average stress ratio α equal to 0.5, whereas the aging of the series nMOS transistors strongly differs: α ranges from 0.125 for MN1 to 0.5 for MN3. As an example, consider the input pattern (1,1,0) (seventh row in Table I). Input voltages of MN1 and MN2 are high ($V_{IN1} = V_{IN2} = V_{dd}$), but also their respective source nodes are at a high voltage (equal to $V_{dd} - V_{th}$), since MN3 is OFF. As a result, $V_{GS1} = V_{GS2} = V_{th}$ and, according to (1), MN1 and MN2 undergo a recovery condition. As for the stress/recovery condition for the transistor MN2 when the input pattern 010 is applied (denoted by x in the table), it depends on the previous input pattern. We can approximate x=0.25, leading to $\alpha = 0.281$ for MN2. The performed analysis can be easily extended to 4-input NAND, and dual results hold true for NOR gates.

Figure 5 depicts the trend over time of the normalized static power (NP_{st}) for both NAND (a) and NOR (b) gates with a number of inputs ranging from 2 to 4. As normalization factors, the respective P_{st0} values have been considered. Since the leakage current depends on input values, we report the trends of the average values obtained considering input

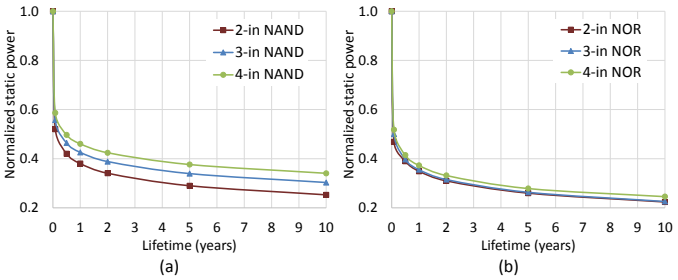


Fig. 5. Profile over time of the static power for 2-to-4-IN CMOS gates ($T_A = 75^oC$): (a) NAND ($P_{st0} = 2.648nW$, $2.312nW$ and $1.755nW$, respectively); (b) NOR ($P_{st0} = 2.399nW$, $1.956nW$ and $1.401nW$, respectively).

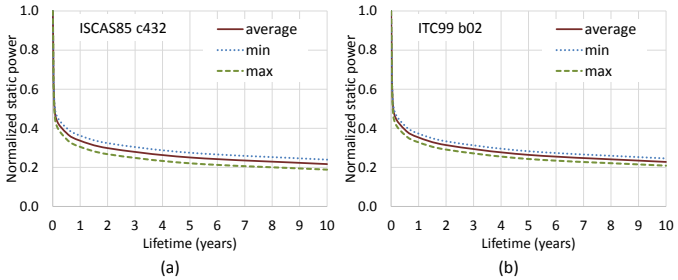


Fig. 6. Profile over time of the normalized static power for the (a) ITC99 b02 and (b) ISCAS85 c432 benchmarks (normalization factors for the average case: $P_{st0}(c432) = 606.4nW$; $P_{st0}(b02) = 74.84nW$; $T_A = 75^oC$).

patterns as equally likely. As can be seen, NP_{st} reduces slightly faster for NOR gates, reaching approximately $0.5P_{st0}$ after only 1 month, and approaching $0.2P_{st0}$ after 10 years. This can be attributed to the cumulative contribution of the aging of the pMOS transistor, which are in series in NOR gates and experience a larger degradation than nMOS transistors. Moreover, a bigger variability with the number of input is exhibited by NAND gates.

TABLE II
STATIC POWER REDUCTION OVER TIME ($T_A = 75^oC$).

Circuit	P_{st0} (μW)	Reduction (%)					
		1m	6m	1y	2y	5y	10y
c499	1.198	53.09	62.86	66.85	70.67	75.51	78.94
c1355	1.443	50.45	60.63	64.63	68.50	73.46	77.01
c6288	6.386	54.36	62.90	66.92	70.78	75.67	79.14
c7552	11.30	52.41	62.53	66.51	70.34	75.20	78.65
s38418	85.39	52.07	62.16	66.15	69.99	74.88	78.36
b18	358.8	50.71	60.87	64.88	68.74	73.68	77.23
b20	61.49	50.50	60.69	64.68	68.53	73.45	76.99
Average	75.15	52.15	61.95	65.95	69.79	74.69	78.17

B. Aging Benefits Evaluation for Benchmark Circuits

We evaluate the reduction of static power due to BTI aging also for benchmark circuits by means of HSPICE simulations. In order to properly account for the effect of BTI aging on static power consumption, we have developed the simulation flow depicted in Figure 4. For the *aged library characterization*, we consider a given workload to compute the stress ratio α for each transistor composing a basic gate in accordance to the considerations given in Section IV-A. The average stress ratio α_{tot}^{ik} for each transistor i in each gate k composing the considered circuits is computed as the average value over all input patterns. It is given by:

$$\alpha_{tot}^{ik} = \left(\sum_{j=0}^{N_{in}} \alpha_j^{ik} P(j) \right) / N_{in}, \forall (i,k), \quad (5)$$

where α_j^{ik} is the stress ratio induced on transistor i of the gate k by the input configuration j, which occurs with probability $P(j)$, N_{in} is the number of input patterns.

Once all stress ratio values are computed and properly included in the aged library, we simulate the circuits for different lifetimes to evaluate the P_{st} trend over time. P_{st} is computed as the average value considering the same workload as for stress ratio estimation. For this analysis, a workload consisting of 1000 random input patterns has been utilized. In this regard, it should be noticed that the correct stress ratio determination would require the awareness of the actual workload. Nevertheless, although this inaccuracy might lead to a wrong estimation of the impact of BTI aging on propagation delay, which is a local effect involving a limited number of gates within critical paths, as far as static power consumption is concerned, the results turns out to be accurate for the purpose of this analysis. Indeed, since static power consumption is an overall figure involving all the gates in the circuit, the stress ratio discrepancies between different transistors compensate.

In Figure 6, we show the results for *b02* and *c432* circuits from the IWLS05 benchmark suite. The solid lines represent the average P_{st} trend over time per input configuration, whereas the dashed lines depict the trend exhibited when it is applied the input pattern giving rise to either the minimum or maximum static power reduction. The differences between the average and the two extreme cases are very small (lower than 3%), confirming the considerations given above. For both circuits, the P_{st} reduction approaches 80% over 10 years.

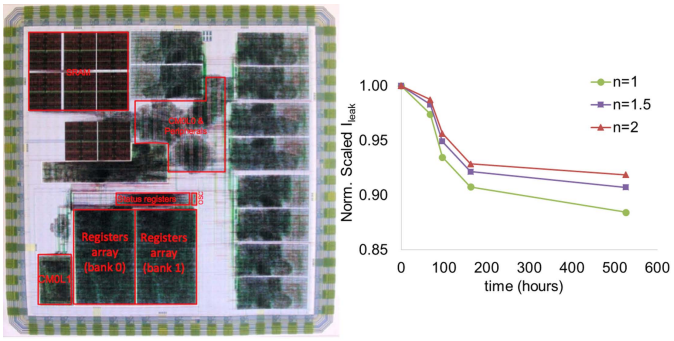
We further assess the aging benefits considering several bigger benchmarks from IWLS05 benchmark suite. The obtained results are reported in Table II. The second column present the values of the P_{st} exhibited at $t0$ for each circuit, which have been utilized as normalization factors. The results presented in columns 3 to 8 confirm those for NOT chain and the *b02* and *c432* benchmarks. After only one month of operation, the static power reduction exceeds 50% of P_{st0} for all considered benchmarks. The average reduction approaches 66% after one year and exceeds 78% over ten years of operation.

C. Experimental Measurements

The BTI aging benefit on static power consumption is confirmed by the experimental measurements that we have performed. Particularly, we have measured actual I_{leak} using a test-chip manufactured with TSMC 65nm technology. Its design floorplan is depicted in Figure 7(a). The V_{dd} of the test-chip is connected to 1.2V power supply through a Digital Multimeter (DMM), whose range and resolution are set to 200uA and 0.1uA, respectively. The leakage current of the test-chip is measured by the DMM in the clock gated domain consisting of processor (CM0L1) and two banks of registers.

TABLE III
MEASURED LEAKAGE CURRENT

Meas. i	1	2	3	4	5
Lifetime (h)	0	68	96	162	526
Temperature (^oC)	59.3	60.0	60.5	60.5	61.3
I_{leak} (μA)	30.4	31.1	30.9	30	30.9



(a) (b)

Fig. 7. (a) Test-chip floorplan; (b) normalized measurements results.

Consider that we have no reliable data on chip actual aging at the beginning of our experiment. Moreover, the resolution of the multimeter employed in our experiment does not allow us to measure the leakage current with the desired accuracy. Table III reports the obtained measurement results. It should be noted that the different chip temperatures during measurements have a big impact in the determination of the actual I_{leak} values. Particularly, I_{leak} increases with temperature. Similarly to [19], in order to highlight the I_{leak} relative reduction over time as a function of BTI aging, and suppress the fluctuation induced by different measurement temperatures, we have normalized the obtained data by a factor derived from (3). Denoting by I_{leak-i} and T_i (with $i = 1 \ldots 5$) leakage current and chip temperature at the $i-th$ measurement, respectively, the normalization and scale factor NSF_i is:

$$NSF_i = I_{leak-1} e^{\frac{qV_{th}(T_i - T_1)}{nkT_1T_i}} \left(\frac{T_i}{T_1}\right)^2, \text{with } i = 1 \ldots 5.$$

The normalized data are plotted in Figure 7(b) for different values of the parameter n in (3) [16]. A clear I_{leak} decrease over time is exhibited, which is in the range 8.1%-11.4% after 526 hours of operation, depending on the value of parameter n. This decrease, however, is smaller than that found by simulation using a 32nm CMOS technology. In this regard, it should be considered that circuits implemented with smaller technology nodes usually exhibit a larger BTI aging degradation [2] and, as a consequence, a more evident leakage current reduction over time.

V. CONCLUSIONS

In this paper, we have shown that BTI aging comes together with considerable benefits for static power consumption P_{st}, due to sub-threshold leakage current reduction. Indeed, P_{st} reduces by more than 50% after only one year of operation, by more than 74% after 5 years. Static power reduction approaches 80% over 10 years of operation. As a result, CMOS designs become more energy efficient over time, and this beneficial effect is expected to increase for more scaled technologies. At the design phase, this reduction must be taken into account to carry out a proper power and thermal analysis.

ACKNOWLEDGMENTS

This work is supported by EPSRC (UK) under grant no. EP/K000810/1 and by the Department of Electrical Engineering and Electronics, University of Liverpool, UK.

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