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A 0.05 mm², 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS

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***Abstract*—In this brief, we present a fully-integrated ring-oscillator based CMOS temperature sensor for Internet-of-Things. Our design relies on a low-complexity PMOS-based sensing circuit to convert temperature into two sub-threshold biasing currents. These are then used to define two oscillation frequencies, whose ratio increases linearly with the temperature. Change in the frequency ratio is finally translated into a digital output code. The proposed sensor was fabricated in 180-nm CMOS technology. When powered at 350 mV, it can achieve an energy/conversion of 0.46 nJ in a conversion time of 33 ms. Moreover, it exhibits a measurement resolution of 0.27 °C and a resolution figure-of-merit as low as 0.034 nJ °C².**

***Index Terms*—CMOS-based temperature sensor, low-voltage, low-power, ring oscillator, real-time sensing.**

I. Introduction

In recent years, we have witnessed an exponential spread of portable, battery-powered devices that sense the surrounding environment and communicate wirelessly the acquired data after some data processing, recognition, and/or classification. Collectively identified as Internet-of-Things (IoT), such devices share the need for reduced power consumption (e.g., in the order of few mW) [1]. Scaling power supply voltage, even down to (or near to) sub-threshold voltage levels, provides the opportunity to design IoT devices with nearly-minimum energy consumption [2]–[4]. Moreover, reducing the die size is a highly sought-after feature for low-cost system integration.

Temperature sensors are widely used in many applications, such as the thermal control and management of processors or systems on chip (SoCs) [5]–[8], ambient temperature monitoring [9], and biomedical devices [10], [11]. Also, they are very popular in IoT devices [12]–[17], where a power consumption of few nW for effective battery life extending is traded-off against a moderate resolution of a few °C.

Several mechanisms to sense temperature were proposed in literature [18]. In a CMOS process, the most established approach consists of exploiting the temperature-dependent characteristics of built-in voltages in parasitic bipolar transistor (BJT) junctions [6], [14]. Afterwards, a digital representation of temperature is obtained by an analog-to-digital converter (ADC). In this way, temperature accuracy of less than ±0.1 °C in a wide temperature range (from –55 °C to 125 °C) with only one-point calibration can be achieved [19]. However, such an approach requires large supply voltages (typically >1 V) and consume µW of power [14]. Resistors are a possible alternative to BJT-based sensors, although the sensing elements tend to be considerably area-hungry [20].

As shown in [15], MOSFET-based temperature sensors potentially allow for a better energy efficiency than above solutions at the expense of lower accuracy and more complex calibration procedures. This class of circuits usually exploit MOSFETs in sub-threshold regime as sensing elements to enable compact sub−1 V/1 µW temperature sensing designs [12]–[15], [21], useful for many practical IoT applications where accuracy and resolution specs can be relaxed.

This brief introduces an ultralow-voltage (0.35 V) fully-integrated CMOS temperature sensor, suitable for energy-constrained IoT applications. A low-complexity PMOS-based sensing circuit is exploited to convert environmental temperature into two sub-threshold biasing currents, used to define two oscillation frequencies whose ratio increases linearly as the temperature rises. The change in the frequency ratio is then translated into a digital output code, through digital back-end based on binary counters. The sensor was fabricated in 180-nm CMOS, with a small silicon area footprint of less than 0.05 mm². When powered at 350 mV, the proposed circuit consumes a power of only 14 nW at 25 °C, while exhibiting an energy per conversion of just 0.46 nJ. Such results were achieved while maintaining an acceptable inaccuracy in the range of ±3 °C (for a typical RMS inaccuracy of 1.2 °C) and a resolution lower than 0.3 °C in the 0 °C – 100 °C temperature range.

The remainder of the paper is organized as follows. Section II details the proposed temperature sensor. Section III presents measurement results over 9 test chip samples. Section IV compares our design with some recent CMOS-based competitors proposed in the literature. Finally, Section V concludes the work.

II. Proposed Temperature Sensor

As shown Fig. 1, and similarly to the approach discussed in [14], our design consists of three main sub-circuits: 1) a temperature-to-current converter (TCC), 2) a current-to-frequency converter (CFC), and 3) a frequency-to-digital converter (FDC). The TCC senses the actual temperature while

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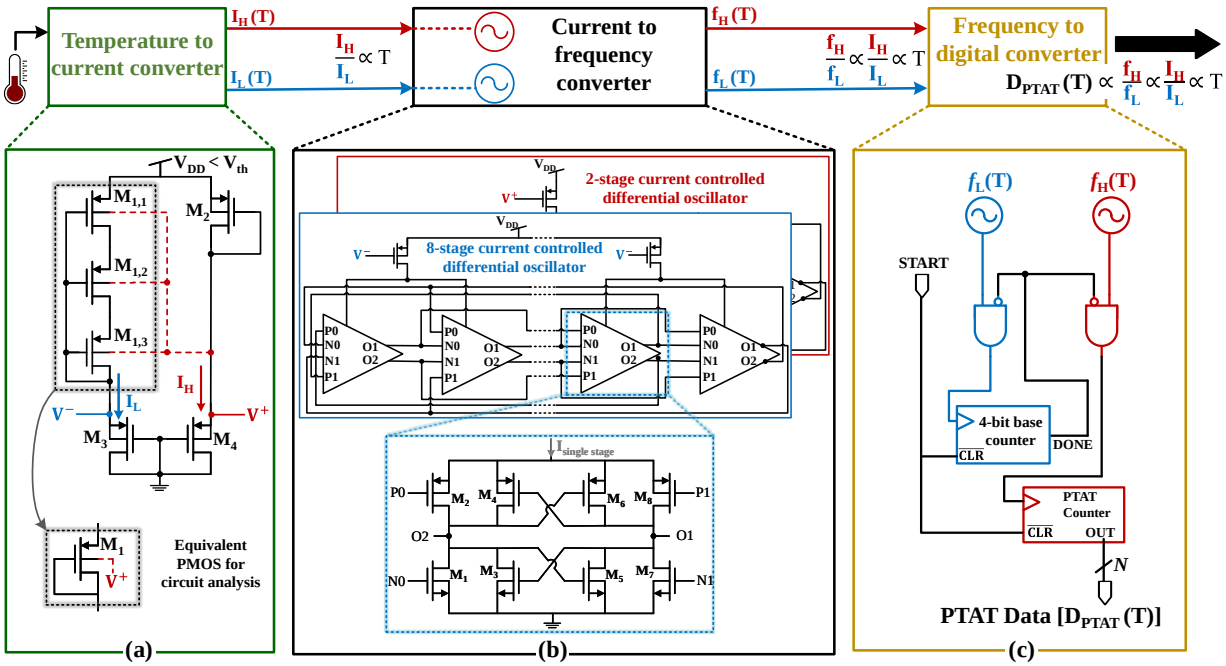

Fig. 1: Block diagram of the temperature-to-digital converter: (a) the temperature-to-current converter (TCC), (b) the current-to-frequency converter (CFC) and (c) the frequency-to-digital converter (FDC).

producing two sub-threshold currents (I_L, I_H), where the current ratio I_H/I_L shows a proportional to absolute temperature (PTAT) behavior in the target temperature range from 0 °C to 100 °C. Such currents are then linearly converted into two frequencies (f_H, f_L) by two current starved differential ring oscillators implementing the CFC. Finally, the FDC generates the digital PTAT (DPTAT) output code, based on the f_H/f_L frequency ratio. All these blocks are detailed in the following.

A. Temperature to Current Converter

As a key point of the adopted temperature sensing scheme, two currents I_H and I_L (with $I_H > I_L$), whose ratio I_H/I_L exhibits a linear PTAT behavior in the target temperature range, need to be reliably generated. This can be achieved by the two-branch TCC circuit shown in Fig. 1(a), where series-connected PMOS diodes are used to define sub-threshold currents with the above property. To gain a deeper insight, the TCC can be simplified by lumping the stacked transistors $M_{1,1}$ to $M_{1,3}$ by an equivalent device M_1. Since all the PMOS transistors of the TCC work in the sub-threshold region, with a source-to-drain voltage, V_{SD}, larger than four thermal voltages $V_T = k_BT/q$ (k_B is the Boltzmann constant, T is the absolute temperature, and q is the electron charge), their source current I_S current can be expressed as [22]:

$$I_S = \frac{W}{L} I_0 \, exp\left(\frac{q(|V_{GS}| - |V_{th}|)}{nk_BT}\right) \tag{1}$$

where V_{th} is the threshold voltage, I_0 is the technology-dependent sub-threshold current extrapolated for $|V_{GS}|=|V_{th}|$, W/L is the aspect ratio of the transistor and n is the sub-threshold factor. In (1), the V_{th} depends on V_{SD} (through the drain induced barrier lowering (DIBL) effect) and on the source-to-bulk voltage V_{SB} (through the body effect) [22].

By considering the upper part of the TCC circuit, the $V^+ - V^-$ voltage can be expressed as:

$$V^+ - V^- = \Delta V_{th} + \frac{nk_BT}{q} \ln\left(\frac{I_L/\left[\frac{W}{L}\right]_1}{I_H/\left[\frac{W}{L}\right]_2}\right) \tag{2}$$

where $\Delta V_{th} = |V_{th1}| - |V_{th2}|$.

If M_3 and M_4 are identical (i.e., $[W/L]_3 = [W/L]_4$ and $V_{th3} = V_{th4}$), the $V^+ - V^-$ voltage can be also expressed as a function of the currents flowing through M_3 and M_4 as:

$$V^+ - V^- = \frac{nk_BT}{q} \ln\left(\frac{I_H}{I_L}\right). \tag{3}$$

Finally, by equating (2) and (3), the final current ratio I_H/I_L expression can be obtained:

$$\frac{I_H}{I_L} = \sqrt{\frac{\left[\frac{W}{L}\right]_2}{\left[\frac{W}{L}\right]_1}} \, exp\left(\frac{\Delta V_{th} q}{2nk_B} \cdot \frac{1}{T}\right). \tag{4}$$

It is worth noting that in (4), ΔV_{th} is constant with temperature despite $|V_{th1}|$ and $|V_{th2}|$ having a complementary to absolute temperature (CTAT) behavior, since $|V_{th1}|$ and $|V_{th2}|$ decrease with the same linear dependence with the temperature. When $|\Delta V_{th}|$ is above 70 mV, equation (4) is well approximated by its linearization in the target temperature range. This is shown in Fig. 2 for $|\Delta V_{th}|$= 88 mV. To achieve such a value, the body terminal of the stacked transistors $M_{1,1}$ to $M_{1,3}$ can be connected to V^+ node. This helps to reach the required ΔV_{th}, while using only PMOS devices of the same transistor type. As reported in Fig. 2, the adjusted R^2 value [14] of the simulated I_H/I_L is 0.9998 in the 0 °C – 100 °C temperature range, thus confirming the required linearity in the response of the designed TCC circuit.

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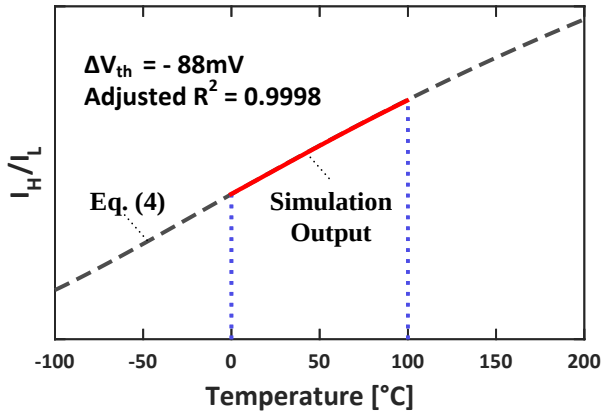

Fig. 2: Temperature-sensing mechanism.

B. Current to Frequency Converter

As shown in Fig. 1(b), the CFC consists of two- and eight-stage current controlled differential oscillators, biased by a mirrored version of the I_H and I_L currents, with oscillation frequency f_H and f_L (with $f_H > f_L$), respectively. Note that the differential delay cell is inherited from the design presented in [23]. The inputs of the delay cell are provided for the NMOS (M_1, M_7) and the PMOS (M_2, M_8) transistors. In order to make negligible the impact of rising/falling slopes on the oscillation frequency, the NMOS inputs are provided by the outputs of the previous delay stage while, those of the PMOS devices come from the outputs of an even earlier delay stage [23]. Then, the NMOS/PMOS (M_3, M_5)/(M_4, M_6) cross-coupled pairs allow to quickly restore the logic levels at the output of the inverters while speeding-up the switching stage [23].

In this way, the oscillation frequency results to be nearly linear with the sub-threshold current of the oscillator I_{bias} and it can be approximated by [23]:

$$f_{osc} = \frac{1}{2N\tau} = \frac{I_{bias}}{2NC_LV} \tag{5}$$

where N is the number of the delay stages, τ is the delay time in a single stage, V is the oscillation amplitude, and C_L is the load capacitance. The two differential oscillators have been designed with a proper number of stages and delay stage sizing, leading to an overall improve of the resolution in the f_H/f_L ratio.

C. Frequency to Digital Converter

The generated frequencies f_H and f_L are then converted into a digital PTAT output through 2 asynchronous counters, as shown in Fig. 1(c). The 4-bit basic counter is used to further increase resolution of the temperature sensor (essentially, it divides by 8 the f_L frequency). The PTAT counter (driven by f_H frequency) has 11 bits. The PTAT counter size is chosen to prevent counting overflow over the temperature detection range from 0 °C to 100 °C, also considering undesired offsets due to process variations. When the $START$ signal is triggered, the oscillators start running and both counters begin counting upward. The counters stop when the fourth bit of the base counter goes to logic 1 (i.e., eight cycles of the slower oscillator have been counted), thus setting the $DONE$ signal. At this time, the temperature-related digital code can be read from the PTAT counter. The counters are reset by the $START$ signal when a new temperature measurement is required.

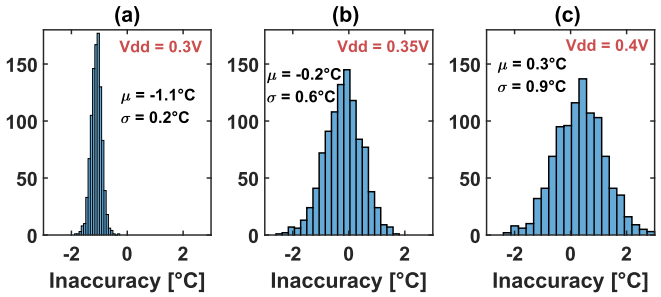

Fig. 3: Inaccuracy at T = 30 °C, as evaluated by 1000 MC simulations for V_{DD} = (a) 0.3 V, (b) 0.35 V and (c) 0.4 V, respectively.

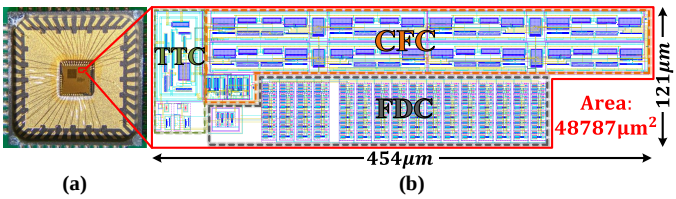

Fig. 4: Micrograph (a) of the testing chip and layout (b) of the proposed temperature sensor.

D. Monte Carlo analysis

Fig. 3(a)-(c) show the deviation (i.e., the inaccuracy) of the digital output of our sensor with respect to the reference calibrated transfer-characteristics (obtained using 10 °C and 90 °C as calibration points), when temperature is 30 °C. In particular, data are extracted by 1000 Monte Carlo (MC) simulations for V_{DD} = (a) 0.3 V, (b) 0.35 V and (c) 0.4 V, respectively. It can be observed that the expected inaccuracy is within the acceptable range of about ± 3 °C for the reference temperature of 30 °C.

III. Measurement Results

The proposed temperature sensor is fabricated in 180-nm CMOS, while occupying a very small silicon area (less than 0.05 μm^2). A die photo of the chip is shown in Fig. 4(a), whereas the circuit layout is detailed in Fig. 4(b). The temperature sensing core (i.e. the TTC) occupies only 4662 μm^2, while the CFC and the FDC circuits occupy 24928 μm^2 and 17029 μm^2, respectively. Measurements were performed on 9 dies. When V_{DD}= 0.35 V and as the temperature spreads from 0 °C to 100 °C, the frequencies of the two differential oscillators were found in the range of few hundreds of Hz and few tens of KHz for the slow and the fast oscillator, respectively. Each sample has been independently calibrated, by exploiting a two point-calibration using 10 °C and 90 °C as reference temperatures. Fig. 5(a) shows the digital output produced by each sample versus temperature, along with the corresponding calibrated transfer-characteristics, demonstrating good linearity: RMS adjusted R^2 value equals to 0.9989, slightly degraded with respect to the simulation value reported

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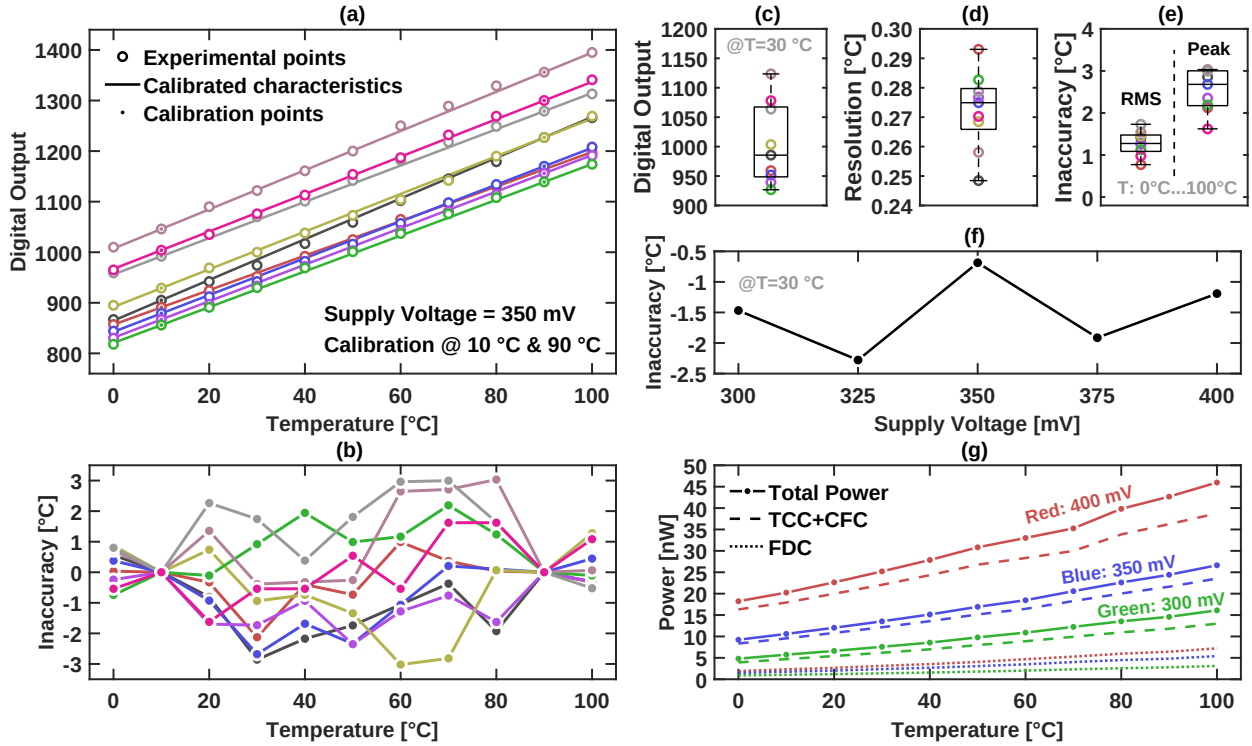

Fig. 5: Measured (a) digital output and (b) corresponding inaccuracy extracted after two-point calibration as a function of the temperature in the 0 °C, 100 °C range, V_{DD} = 350 mV. Die-to-die variability box plots of (c) digital output at 30 °C, (d) temperature resolution (inverse slope of calibration curves in (a)) and (e) inaccuracy (RMS and peak errors). Measured (f) line sensitivity at 30 °C as a function of the supply voltage and (g) power consumption of temperature-to-current converter (TCC), current-to-frequency converter (CFC) and frequency-to-digital converter (FDC) as a function of temperature. (f) and (g) are extracted on a single reference sensor.

TABLE I
COMPARISON WITH STATE-OF-THE-ART

	JSSC'14 [21]	JSSC'16 [7]	TCASII'19 [8]	JSSC'19 [15]	JSSC'19 [14]	ISSCC'17 [16]	TCASI'21 [17]	This work
Technology	180nm	65nm	180nm	65nm	180nm	180nm	130nm	180nm
Supply Voltage [V]	1.2	1	0.9	0.5	0.8	1.2	0.95	0.35
Area [mm^2]	0.09	0.008	0.007	0.63	0.074	0.22	0.07	0.049
Measured Samples	18	7	3	12	9	16	9	9
Temperature range [°C]	0 -100	0 -100	0 -100	0 -100	-20 - 80	-20 - 80	0-80	0-100
Absolute Inaccuracy [°C]	-1.4/1.5	-0.9/0.9	-1.64/0.67	-1.53/1.61	-0.9/1.2	-0.76/0.76	-0.4/0.44	-3/3
Calibration	2-point	2-point	2-point	2 point	2-point	2-point	2-point	2-point
Resolution [°C]	0.3	0.3	0.55	0.3	0.145	90m	0.1	0.27
Conversion Time [ms]	30	0.022	300	300	839	8	59	33
Energy/Conversion [nJ]	2.2	3.4	1.2	0.23	8.9	4.56	11.56	0.46
R-FoM* [nJ·K^2]	0.19	0.3	0.36	0.02	0.19	0.037	0.116	0.034
Power [W]	71n@27°C	154µ@27°C	3.92n@27°C	763p@27°C	11n@25°C	570n	196n@30°C	14n@25°C

* R-FoM = Energy/Conversion × Resolution^2

for the I_H/I_L in Fig. 2. In Fig. 5(b), the inaccuracy is reported for each sample as a function of the temperature. Die-to-die variability is considered in Fig. 5(c-e), reporting the box plots of (c) the digital output produced by each sensor at 30 °C, of (d) the sensor resolution (inverse slope of calibrated transfer-characteristics) and of (e) the inaccuracy, in both RMS and peak terms. Considering the die-to-die deviations obtained for the 30 °C digital outputs (c) and for the resolutions (d) - i.e., vertical offset and inverse slope of transfer-characteristics, respectively - featured by different sensors operated in the same condition, it is clear that the calibration performed on every single device is a strong requirement for our sensor. In fact, for a median resolution of 0.275 °C, a deviation of 50 in the digital output would correspond to an unacceptable inaccuracy higher than 13 °C. However, after calibration, each sensor can benefit from the high resolution (worst case measured value is 0.295 °C) to obtain a reduced inaccuracy (e): the median RMS and peak inaccuracy are 1.2 °C and 3.1 °C, extracted on each sample in the target 0 °C – 100 °C temperature range. Reported values are within the acceptable limits for most of the practical IoT applications and temperature adaptive designs [6]. Additional measurements performed on a single reference sensor are reported in Fig. 5(f-g). In (f), the V_{DD} dependence of temperature inaccuracy has been extracted at 30 °C for the 300 mV – 400 mV supply voltage range. Finally, the power consumption of each block implementing

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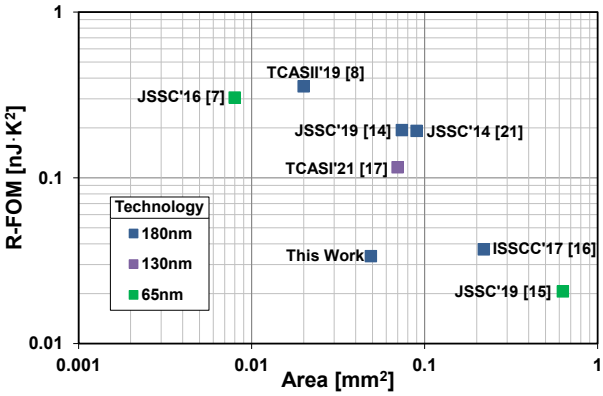

Fig. 6: R-FOM versus area comparison.

the sensor is reported in Fig. 5(g): it can be observed that the power contribution of TCC and CFC over the total power consumption is dominant (about 85% on average). Moreover, the power consumption of the sensor is strongly dependent on the actual temperature, spreading from 9.23 nW at 0 °C to 26.64 nW at 100 °C, for a 350 mV supply voltage. The whole sensor consumes 7.1 nW at 25 °C when operated at 300 mV supply voltage (23.93 nW at V_{DD} = 400 mV).

IV. Comparison

Table I summarizes measurement results of the temperature sensor as compared to prior work, based on CMOS designs. Our design operates at the lowest supply voltage, and achieves competitive resolution and power consumption at the expense of accuracy, which however remains within an acceptable range (i.e., ±3 °C) for various IoT and temperature adaptive applications. The proposed sensor exibits a very competitive resolution figure-of-merit (R-FoM), defined as $Energy/Conversion \times Resolution^2$ [18]. This is achieved in spite of its reduced silicon area occupation, as shown in Fig. 6. In particular, our design results to be the second best in terms of occupied silicon area and the absolute best in terms of R-FoM among the sensors designed in CMOS 180-nm. Such features make the proposed sensor very attractive to be integrated in battery-powered low-cost IoT devices.

V. Conclusion

This paper demonstrated an ultralow-power, fully-integrated temperature sensor suitable for energy-constrained, low-cost applications. The circuit was fabricated in 180-nm CMOS technology, while exhibiting a compact footprint (i.e., less than 0.05 mm^2). When operated at 0.35 V, the sensor consumes 14 nW at 25 °C, and achieves a competitive resolution of 0.27 °C in the temperature range from 0 °C to 100 °C, after 2-point calibration. Notably, our design can achieve an energy/conversion of only 0.46 nJ with a conversion time of just 33 ms.

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