Sub-Parts Per Million NO_2 Chemi-Transistor Sensors Based on Composite Porous Silicon/Gold Nanostructures Prepared by Metal-Assisted Etching

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Abstract

Surface doping of nano/meso-structured materials with metal nanoparticles to promote and optimize chemi-transistor sensing performance represents the most advanced research trend in the field of solid-state chemical sensing. In spite of the promising results emerged by metal-doping of a number of nanostructured semiconductors, its applicability to silicon-based chemi-transistor sensors has been hindered so far by the difficulties in integrating the composite metal-silicon nanostructures using the complementary metal-oxide-semiconductor (CMOS) technology.

Here we propose a facile and effective top-down method for the high-yield fabrication of chemi-transistor sensors making use of composite porous silicon/gold nanostructures (cSiAuNs) acting as sensing gate. In particular, we investigate the integration of cSiAuNs synthesized by metal-assisted etching (MAE), using gold NPs as catalyst, in solid-state junction-field-effect transistors (JFETs), aimed at the detection of NO_2 down to 100 parts per billion (ppb). The chemi-transistor sensors, namely cSiAuJFETs, are CMOS compatible,

operate at room temperature, and are reliable, sensitive, and fully recoverable for the detection of NO_2 at concentrations between 100 and 500 ppb, up to 48 h of continuous operation.

1. Introduction

Detection of NO_2 has become increasingly marked for environmental control and personal safety because of its dangerous effects on human health and environment, and its large emission from on-road vehicle and industrial process exhaust, as reported by the European Environment Agency (EEA). [1] This fact leads to stringent regulatory laws and controls on exhaust emissions level and composition and, in turn, to the need for miniaturized sensors with low limit of detection, high sensitivity, high throughput, with small cross-sensitivity, for a reliable detection of NO_2 at concentration as low as 53 ppb. [2]

Commercial NO_2 sensors are typically chemi-resistive and make use of semiconducting metal oxides, such as tin oxide (SnO_2), tungsten oxide (WO_3), or zinc oxide (ZnO). Although they do show excellent sensitivity, limit of detection is typically 1 ppm and operation temperature is in the range of 200–600 °C. [3] Challenges are reduction of the power consumption due to the high operation temperature, as well as improvement of the limit of detection.

Because of their amplified response, lower-temperature operation, and tunable sensitivity, with respect to chemi-resistor sensors, chemi-transistor sensors [4] [5] have led to extensive research and their impact can be easily envisaged from analysis of markets related to health-care, environment-control, food-safety.

Moreover, chemi-transistor sensors based on nano/meso-structured materials have demonstrated to outperform their standard counterpart making use of bulk materials. This is due to the higher surface-area and higher chemical-affinity of materials at the nano/meso-scale that allow a more effective interaction with molecules coming from the surrounding environment. Examples are carbon nanotubes [6], graphene [7], porous silicon (PS) [8], metal-oxide nanowires [9], organic polymers [10], and silicon nanowires [11] [12].

Remarkably, surface doping of these nano/meso-structured materials to promote and optimize the chemi-transistor sensing characteristics represents a significant advance in the field of solid-state chemical sensing. Excellent works concerning the modification of flat [13] and nano/meso-structured semiconductors via surface decoration with both metal and metal-oxide nano-clusters/particles with size- and shape-dependent physicochemical properties have been reported for metal-oxides [14], carbon nanotubes [15], III-V semiconductors [16]. Commonly exploited dopants for the detection of NO_2 and nitrogen oxide (NO), namely NO_x, include noble metals such as Pb, Pt, Ag and Au nanoparticles (NPs), owing to their privileged catalytic properties and distinctive selectivity toward NO_x gases. [14 16 15,17 18] The inclusion of metal nanoparticles on the nanostructured semiconductors leads to the synthesis of composite metal-semiconductor materials with enhanced sensing capabilities achieved by bringing the catalytic properties of the metal nanoparticles and the widely tunable bandgap of the nanostructured semiconductors into play. In such composite materials metal nanostructures act as gateways able to influence the transit of electrons to and from the semiconductor interface onto which they are deposited. This gives rise to large and fast changes in the electrical properties of the sensing material upon interaction with specific analytes, which translate into an improvement of the chemi-transistor response in terms of dynamics, sensitivity, and, more important, of selectivity.

In spite of the promising results emerged by metal-doping of a number of nanostructured semiconductors, its applicability to silicon-based chemi-transistor sensors has been hindered by the difficulties in integrating the composite metal-silicon nanostructures using the complementary metal-oxide-semiconductor (CMOS) technology. Silicon-based chemi-transistors have various advantages over the other nanomaterial-based ones, since the former can exploit well-developed CMOS technology and process to integrate the chemi-transistors into small chips together with control and readout electronics, thus envisaging fabrication of

sensing chips at low cost. As to metal-doped silicon chemi-transistor, only recently a silicon-nanowire chemi-transistor decorated with Pd nanoparticles has been reported for H_2 sensing. [19] Here we propose a facile and effective top-down method for the high-yield fabrication of chemi-transistor sensors making use of composite porous silicon/gold nanostructures (cSiAuNs) acting as sensing gate. In particular, we investigate the integration of cSiAuNs synthesized by metal-assisted etching (MAE), [20-21] using gold NPs as catalyst, in solid-state junction-field-effect transistors (JFETs), aimed at the detection of NO_2 down to 100 parts per billion (ppb). The chemi-transistor sensors, namely cSiAuJFETs, operate at room temperature and are reliable, sensitive, and fully recoverable for the detection of NO_2 at concentrations between 100 and 500 ppb, up to 48 h of continuous operation. We argue that adsorption of NO_2 on the cSiAuN surface modifies the fixed charge of cSiAuNs by efficiently depleting of free electrons the silicon nanostructure via gold nanoparticle mediation and, in turn, modulating the width of the space-charge region at the cSiAuN/JFET-channel interface. This accounts for the fast and reliable variation of the sensor current at such low NO_2 concentrations. Moreover, the possibility of tuning the thickness and to control the morphology of the composite porous silicon/gold nanostructures is also investigated, thus envisaging versatile physical and chemical properties of this material as sensing gate toward the detection of NO_2.

To the best of our knowledge, the use of MAE for the integration of nanostructured silicon/metal composites into chemi-transistor sensors has not been reported so far and represents a great potential for the fabrication of metal-doped (e.g. using Au, Ag, Pt) silicon-based chemi-transistors with peculiar sensing features, in terms of sensitivity and selectivity, towards specific gases. In fact, while significant efforts have been devoted to energy conversion application of silicon nanostructures prepared by MAE, [22 23] only one work on their gas sensing property has been reported using a chemi-resistor sensor.[24]

2. Synthesis and characterization of composite porous silicon/gold nanostructures (cSiAuNs)

Synthesis of composite porous silicon/gold nanostructures using MAE is thoroughly investigated by chemical etching of silicon in HF/H_2O_2 solution activated by gold nanoparticles deposited on the Si surface by electron-beam assisted thermal evaporation, as given in the literature [25] [26-27]. A systematic study is carried out on p and p^+ silicon so as to investigate influence of nominal gold-thickness and etching-time on both morphology and pore depth of the resulting cSiAuNs versus silicon resistivity.

It is well known that by properly tuning thermal evaporation parameters, e.g. temperature, partial pressure, thickness and deposition rate, for nominal thickness in the nanometer range the metal film coating gives rise to a surface coverage not fully connected and forms metal nanoparticles or nano-islands that have similar distribution density and size, thus leaving sections of the silicon surface free from metal. [28-30] With all the other parameters fixed, the features of metal-NPs are deeply dependent on the nominal thickness of the film deposited, which, in turn, is deeply affecting the resulting etched silicon nanostructure. Size, shape, and distribution of the gold NPs change as the nominal thickness of the evaporated gold film increases, from a few isolated nanoparticles of spherical shape with uniform distribution, to partially interconnected patches of elongated NPs which tend to coalesce and form clusters. [31] According to the commonly accepted mechanism for MAE of silicon, [25, 27] after immersion of the samples in solution of HF and H_2O_2, gold NPs rapidly sink into the Si bulk following the main crystallographic direction (100) of the silicon substrate, thus creating as a result pores in the Si substrate or, additionally, Si wires. The reaction mechanism consists in the reduction of H_2O_2, promoted by metal clusters, and the oxidation of Si, subsequently etched by F^- ions. Due to the catalytic activity of metal, holes (h^+) from the reduction of the oxidative agent are injected into the valence band of silicon, therefore causing the Si etching right underneath the

metal clusters because of the much faster etching of the Si under metal catalyst than Si without metal coverage. [32-33]

Figure 1-a,b,c shows Scanning Electron Microscope (SEM) images of different composite porous silicon/gold nanostructures (cSiAuNs) obtained from silicon samples coated with different nominal gold-thickness films, namely 0.7, 1.5 and 3 nm, and etched for a fixed time of 90 s.

Firstly, we observe that morphology of pores and diameter of pillars of the cSiAuNs resulting from the MAE process significantly depend on the nominal thickness of the metal film deposited on top of the silicon surface and, in turn, on the size and distribution of the Au NPs evaporated. In our experiments, namely 0.7 nm-thick Au coating on the silicon surface corresponds to a low distribution density of the metal NPs, which leads to low porosity cSiAuNs with vertical pores separated by crystalline silicon pillars with size comparable to the pore diameter (Figure 1-a). Lift-off or Brownian movement of the metal NPs may occur during the silicon dissolution in the case of thin film thickness, therefore contributing to the formation of non-columnar silicon nanostructures. [34-35] On the other hand, thicker metal films of 1.5 nm lead to higher NP density and, consequently, to higher porosity cSiAuNs with columnar morphology, where pores are separated by thin silicon pillars with more uniform cross-sectional shape and height (Figure 1-b). According to the literature [36], by further increasing the metal thickness up to 3 nm and, in turn, the density of NPs, both porosity and aspect ratio of the resulting cSiAuNs are increased, up to the formation of silicon nanowires (SiNWs). In fact, deposition of thicker gold layer through thermal evaporation leads to the formation of non-uniform NPs with higher distribution density that tend to coalesce and form clusters. [31] The resulting etched nanostructures consists on thin walls of Si (the nanowires) that tend to collapse in triangular shape inclined of 38° (Figure-1-c). [31] A clustering at the silicon wire tips due to critical forces acting at the meniscus between air and pentane during the final drying step is observed. [29]

Further characterization is performed on cSiAuNs obtained from the 1.5 nm-thick Au coating (Figure 1-b) because of both its larger specific surface area compared to the composite nanostructures obtained from 0.7 nm-thick Au coating (Figure-1-a), and its higher fabrication reliability in terms of mechanical stability compared to the composite nanostructures obtained from 3 nm-thick Au coating (Figure 1-c).

Figure 1-d, e, f shows SEM images of cSiAuNs obtained with 1.5 nm-thick Au coating and etched at different times in a range of 30 to 90 s, with a step of 30 s. By tuning the etching time we are able to control the composite porous silicon/gold nanostructure thickness. cSiAuNs maintain the same well defined homogeneous columnar morphology while the thickness of the layer linearly increases in a range from 680 nm to 2 μm, from 30 to 90 s, due to the further sinking of metal nanoparticles upon prolonged immersion in the HF/H_2O_2 solution.

The relationship between cSiAuN main parameters, namely pore depth, Au thickness, and etching time is summarized in **Figure 1-g, h**, which reports silicon pore-depth as a function of Au-thickness coating and of etching time, respectively. Figure-1-g shows that cSiAuN layers exhibit a depth from 1.2 μm to about 2 μm, when Au thickness varies from 0.7 nm to 3 nm. In particular, the increase of metal layer thickness from 0.7 to 1.5 nm determines a steep increase of nanostructure depth, which reflects an augmented etching rate as the nominal metal thickness changes from 0.7 to 1.5 nm. This augmented etching rate is due to the increasing physical access of the etchant to the area [31] underneath Au nano-islands (active site), which is related to the increase of grain size and coalecence of gold NPs and, in turn, determined by the augmented thickness of metal film deposited. [21, 37] By further increasing Au thickness, cSiAuN depth becomes slightly dependent on both size and distribution of metal NPs and the depth-thickness curve tends to saturate around 2 μm of pore depth (Figure 1-g). Such a behavior can be explained by considering that the catalytic activity of Au nanoparticles has been demonstrated to be very sensitive to the ratio between Au particle size and

Au/semiconductor perimeter interface.[38-39] For clusters in an intermediate size range (Au thickness between 1.5 nm and 3 nm), defect energies from the edge and corner atoms become non-negligible and the ratio between the size of clusters and the perimeter interface is similar, thus leading to the same physical access area to the etchant. Moreover, Figure 1-g also evidences that the catalytic activity of gold NPs is not critically influenced by the doping of silicon on which they are deposited, leading to similar etching rate Au-covered (under identical conditions) regions both on a p+ (0.04 Ω cm) (Figure 1-g, red line) and on a p (2.5–4 Ω cm) (Figure 1-g, blue line) Si substrates that differ from two orders of magnitude in resistivity. [40]

Concerning the relationship between etching rate and doping level, for Au-covered (under identical conditions) regions on p+ (0.04 Ω cm) and on p (2.5–4 Ω cm) Si substrates (Figure 1-h, red line and blue line, respectively), only small variations in pore size and etching depth are observed, according to literature.[41] With all the other parameters fixed, the Au-coated area on the highly doped p+ Si is etched into a columnar porous structure with slightly deeper pores (between 200 and 300 nm higher) but same rate of dissolution (20 nm/s), with respect to the one obtained with low doped p Si (Figure 1-h, blue line). [40]

The presence of gold NPs on the porous silicon matrix is verified by X-ray photoelectron spectroscopy (XPS) analysis of cSiAuNs, also providing information about both composition and oxidation states of the deposited metal NPs and of the nanostructured silicon surface. As shown in **Figure 1-i**, the Au 4f core level spectrum in cSiAuN exhibits a principal component with $4f_{5/2}$ and $4f_{7/2}$ levels at 87.9 and 84.2 eV, respectively. It is interesting to observe the small shift of 0.3 eV in the core-level binding energy in respect to Au foil (for which $4f_{5/2}$ and $Au_{7/2}$ peaks are located at 87.6 and 83.9 eV, respectively) that could be ascribed to quantum size effect of NPs [42]. Two other components located at higher binding energy (one at 88.6 and 85.0 eV and a less intense one at 89.6 and 86.0 eV) can be identified.

These features can be attributed to gold silicide (Au_xSi) in good agreement with literature data [42-44] reporting the formation of intermetallic species Au_xSi with x going from 2 to 7 [45] during AuNP deposition on silicon, composed of Au at different oxidation states that originates several components in the Au 4f spectrum at higher binding energies than that of metallic Au. The experimental ratio between peak areas of the metallic Au and Au_xSi components is estimated to be equal to 5. The presence of Au_xSi species is further confirmed by the analysis of Si 2p signal (data not shown) exhibiting three different components, specifically at 100.0 eV attributable to Si-Si bonds, at 102.4 eV due to the contribution of Si 2p states in gold silicide, and at 103.7 eV attributable to SiO_2. [44]

3. Integration of composite silicon/gold nanostructures into a chemi-transistors platform (cSiAuJFET)

On the basis of the results obtained on the preparation of composite porous silicon/gold nanostructures using different MAE parameters (section 2), cSiAuNs prepared from 1.5 nm-thick Au coating and 90 s etching time are selected for the fabrication of chemi-transistor devices, because of both the larger specific surface area and enhanced fabrication reliability. Through a post-process step based on MAE of the CMOS compatible process-flow, junction-field-effect transistor (JFET) exploiting a cSiAuN layer as extra sensing-gate is fabricated, The resulting chemi-transistor sensor, namely cSiAuJFET, specifically consists of a p-channel JFET in which the cSiAuN layer is selectively integrated on top of the p-channel between source (S) and drain (D) terminals.

Figure 2 shows a schematic representation of the main process steps required for the integration of the cSiAuN into a JFET device. The cSiAuJFET is fabricated on pn-type silicon wafers (nominal resistivity of p-type and n-type silicon layers of 0.04 Ω cm and 2-4 Ω cm, respectively). The metallurgical junction between p- and n-type silicon is located at 2.3 µm from top. The cSiAuJFET sensor is fabricated by defining aluminum source and drain

contacts (both comb-like and parallel-plate in shape) on the silicon substrate. Aluminum deposition is performed both on p-type silicon (front-side surface) and on n-type silicon (back-side surface) (Figure 2-a). Both comb-like and parallel-plate source (S) and drain (D) terminals are defined by patterning (1st mask) the aluminum film on top of the p-type silicon (front-side surface) (Figure 2-b). Source and drain terminals are then protected using a patterned photoresist layer (2nd mask) (Figure 2-c), through which deposition of 1.5 nm-thick gold layer on the p-type silicon between source and drain is performed (Figure 2-d). Selective gold-assisted chemical etching of part of the p-type silicon between drain and source terminals is performed to produce the composite porous silicon/gold nanostructured layer on top of the p-channel, then the patterned photoresist is removed (Figure 2-e). Figure 2-e shows the final structure of the chemi-transistor sensor of this work, which is characterized by two independent gates: a solid electrical gate on the back-side, which allows the current of the JFET device to be electrically tuned, and a nanostructured sensing gate on the front-side, which allows the JFET device to be provided with sensing capability. Figure 2-f shows an SEM cross-section of the typical composite porous silicon/gold nanostructured layer that is integrated between drain/source terminals of the JFETs and exploited for sensing purposes. An overall number of 24 cSiAuJFET sensors with same nominal thickness (1.2 μm) and morphology (columnar-like) of the cSiAuN layer are integrated on the same silicon die over an area of 1 cm^2. The sensors feature same channel length L=100 μm, but different drain/source terminals configuration (parallel-plate and comb-type) and size (effective channel widths W of 300 μm and 1500 μm for parallel-plate configuration, 3000 μm and 7500 μm for comb-type configuration). Figure 2-g shows an optical microscope top-image of different sensor structures with parallel-plate (W=1500 μm) and comb-like (W=7500 μm) drain and source terminals. The cSiAuN (black areas) is clearly visible between source and

drain contacts (white areas). Flat silicon surface (grey areas) not involved into the MAE etching step and defined by the difference of 1st and 2nd patterning masks is also noticeable. The MAE approach allows fabricating a unique chemi-transistor sensor in which the composite porous silicon/gold nanostructured material acts as a sensing gate, which operates independently of the electrical gate of the JFET device. According to the literature, [8] the nanostructured sensing gate operates by modulating the depletion region width x_1 at the cSiAuN/p-channel interface (Figure 2-f) upon adsorption/desorption of analytes on the composite Si/Au nanostructured material itself, thus effectively modulating the p-channel thickness and, in turn, the current flowing in the p-channel dependently on the gas concentration, for a given gate voltage. On the other hand, the electrical gate operates by modulating the depletion region width x_2 at the p-channel/n-silicon interface (Figure 2-f) through electrical tuning of the gate terminal voltage of the JFET, thus effectively changing the p-channel thickness and, in turn, the current flowing in the p-channel independently of the gas concentration.

4. Detection of low concentrations of NO_2 using cSiAuJFET chemi-transistors

For gas sensing performance evaluation, the silicon die integrating cSiAuJFET devices is soldered onto a TO-8 support and placed in a stainless steel chamber. A thorough electrical characterization of the cSiAuJFET sensors is performed in NO_2 in the range 100-500 ppb at room temperature (RT), using flow-through technique, up to 48h of continuous operation. For all the experiments, flow-rate is maintained at 200 standard cubic centimeter per minute (sccm), synthetic air is used as carrier gas, relative humidity is set to zero, and temperature is set to 25±0.5 °C. The cSiAuJFETs are biased in the saturation region (V_{DS}=-2 V) and exposed to synthetic air in the gas chamber for 60 min. This period is necessary to settle the output response of the sensor to a stable current value (warm up period). We argued that desorption of molecules (mostly water with donor-like behavior) adsorbed on the cSiAuN surface during

storage in ambient air occurs in this phase, which leads to a decrease of the positive fixed charge of the cSiAuN material and, in turn, to a reduction of the space-charge width in the p-channel underneath the cSiAuNs and to an increase of the current flowing in the p-channel during the warm up period. Afterwards the sensors are exposed to NO_2 for 30 min (adsorbing phase) and then to synthetic air for 60 min (desorbing phase), repeating the protocol on the entire concentration window (100-200-500 ppb), whereas the gate voltage (0, 0.7, 1.5, 2.5 V) is tuned at the end of each adsorbing phase of 500 ppb. Time exposure has been chosen based on the "The National Institute for Occupational Safety and Health" (NIOSH) according to "Immediately Dangerous to Life and Health" (IDLH) levels, which correspond to concentration of the toxic agent after 30-minute exposure.[2,46]

Figure 3 reports experimental data on the gas sensing performance typical of cSiAuJFETs with parallel-plate source and drain terminals and with channel width W=1500 μm. Experimental data on the gas sensing performance typical of cSiAuJFETs with comb-type source/drain terminals and with channel width W=7500 μm are reported in Figure S1. For completeness, experimental data simultaneously measured on four cSiAuJFETs with both parallel-plate and comb-type drain/source terminals and different channel widths (300, 1500, 3000, 7500 μm) are reported in Figure S2.

Figure 3-a shows a typical time-resolved curve (current versus time) of cSiAuJFET measured upon NO_2 exposure at concentration of 100, 300, 500 ppb for different gate polarization voltages V_{GS} (V_{GS} = 0, 0.7, 1.5, 2.5 V). The drain-to-source current I_{DS} of each sensor exposed to NO_2 gas is continuously measured for two days (up to 48 h) and plotted against time. The total gate current I_G flowing through the gate terminals of all the sensors under measure is also continuously monitored as control, in order to rule out possible contribution of the gate current changes to the sensor response under NO_2 exposure. The I_G maximum value is of several hundreds nA and occurs at the highest gate polarization voltage V_{GS}= 2.5 V, which allows to rule out significant contribution of the gate current when the sensor current I_{DS} is

above 1 μA. For this reason, plots of time-resolved curves are limited to I_{DS} current values above the threshold value of 1 μA.

The sensors show a reliable behavior independently of the gate voltage values, with the sensor current I_{DS} quickly increasing when NO_2 is injected into the test chamber to reach the saturation value in few minutes and then quickly decreasing when NO_2 is removed from to restore the quiescent current value (I_{DS0}) in synthetic air without significant drift. The effect is evident by repeating the protocol up to 48 h. For each sensor, current changes increase as the NO_2 concentration increases for all the tested V_{GS} values. Notably, the sensor behavior is well reliable up to 2 days of continuous operation, independently of the polarization-voltage value V_{GS}.

The current increase after the exposure to NO_2 could be explained by considering that NO_2 behaves as electron acceptor. According to the theory, on the one hand, the increase on the concentration of free-charge carriers (holes) in cSiAuNs (doping effect) due to adsorption of NO_2 leads to an increase of the cSiAuN conductivity and, in turn, of the current flowing through it. [47-48] On the other hand, the decrease of the (positive) fixed charge density of cSiAuNs due to NO_2 adsorption and consequent formation of NO_2^- radicals leads to a reduction of the space-charge width in the p-channel underneath the cSiAuNs and, in turn, to an increase of the current flowing in the p-channel. [49 8]According to the literature,[49 8] while the former mainly accounts for the chemi-transistor current variation at higher V_{DS} values, the latter accounts for the current variation at lower V_{DS} potential values, which is the case of this work. We argue that the small current flowing through the cSiAuNs of the chemi-transistor sensor might account for the non-complete saturation of the cSiAuJFET current in steady-state conditions [50].

Figure 3-b highlights time-resolved responses of the cSiAuJFET sensor in Figure 3-a, for the different NO_2 concentrations and V_{GS} values tested, in a narrower time-window (0 to 1h). On

the one hand, the increase of V_{GS} produces a reduction of the quiescent current in synthetic air I_{DS0} from 120 μA at V_{GS}=0 V to about 4 μA at V_{GS}= 2.5 V. On the other hand, the increase of the NO_2 concentration produces a maximum absolute variation of the sensor current I_{DS} of 20 μA at V_{GS}=0 V and of 7 μA at V_{GS}=2.5 V, for NO_2 concentration of 500 ppb. For all the tested sensors, it is evident that by increasing the V_{GS} value the absolute current variation reduces, whereas the relative current variation of the sensor increases. Rise and fall times are about 5 and 10 minutes, respectively, and only slightly dependent on the values of V_{GS}, accordingly to the literature on nanostructured chemi-transistor sensors based on JFET devices [8] and differently from those based on MOSFET devices. [51 52] No significant variation of rise and fall times are observed up to 48 h of continuous operation.

Figure 3-c reports the relative current variation ΔI_R of the sensor in Figure 3-a,b as a function of the NO_2 concentration (calibration curve). ΔI_R is by definition $(I_{DS} - I_{DS0})/I_{DS0}$ in the saturation region at V_{DS} =-2 V, where I_{DS0} is the quiescent current value in air. For all the tested devices, at fixed NO_2 concentration, ΔI_R non-linearly increases with the V_{GS} value in the range 0 to 2.5 V; at fixed V_{GS} values, ΔI_R linearly increases with the NO_2 concentration in the range 0-500 ppb. Notably, all the sensors feature a linear calibration curve within the range of NO_2 concentrations investigated.

Calculation of sensitivity (S), by definition $S = \partial \Delta I_R / \partial [NO_2]$, is performed by taking the slope of the linear regression curve best-fitting the experimental data of Figure 3-c, for each tested V_{GS} value within the NO_2 window of concentrations tested. Figure 3-d shows the values of sensitivity as a function of the V_{GS} voltage values typical of sensors with parallel-plate drain/source configuration (please, refer to Figures S1b and S1c for comb-type configuration). Experimental data in Figure 3-d are best-fitted with a quadratic curve, which highlight the non-linear dependence of the sensitivity on the V_{GS} voltage, for the case of parallel-plate devices (comb-type devices show a linear dependence of the sensitivity value on the gate

voltage). It is worth noting that, for V_{GS} values between 0 V and 2.5 V the sensitivity of the cSiAuJFET in Figure 3 can be varied of a factor of 5.6 from $2.5x10^{-4}$ ppb^{-1} to $1.4x10^{-3}$ ppb^{-1}, thus demonstrating that tuning of this key parameter can be used to adjust the sensor response in real-time without the need of using wide dynamic-range voltages. A variation of the gate voltage from 0 V to 0.7 V is adequate to scale the value of S of 51.9%. As already reported,[8] this result demonstrates that possible drawbacks of up-to-date gas sensors, such as aging effects and fabrication reliability, can be effectively addressed.

By further comparison of experimental data in Figure 3 and Figure S1 that refer to parallel-plate and comb-type source/drain terminal configurations, respectively, it is apparent that high reliability over time (up to 48 h) (Figures 3-a,b and S1-a,b) and high linearity of the calibration curve (Figures 3-c and S1-c) is achieved for all the tested sensors, independently on both source/drain configuration and W/L ratio. As expected and coherently with the channel width-to-length ratio (W/L) of the fabricated JFET devices, the different sensors feature different I_{DS} current values under exposure to both air and NO_2 (Figures 3-a,b and S1-a,b). For instance, I_{DS} values are in the range of 20 μA (absolute value) for sensors with W= 300 μm, up to 1.8 mA (absolute value) for sensor with W=7500 μm, in air at V_{GS} = 0V. A comparison of time-resolved response curves of four cSiAuJFETs integrated on the same silicon die with different source/drain terminal configurations and different W/L ratios is reported in Figure S2-a.

It is worth noting that, sensors with parallel-plate drain/source configuration (smaller W/L ratio) show higher relative current variation and, in turn, sensitivity value (Figure 3-c), with respect to those with comb-finger configuration (larger W/L ratio) (Figure S1-c). A comparison between calibration curves (ΔI_R versus NO_2 concentration) of four cSiAuJFETs integrated on the same silicon die with different source/drain terminal configuration, at V_{GS}=1.5 V, is provided in Figure S2-b. Moreover, a quadratic dependence of the sensitivity

value on the gate voltage V_{GS} value occurs for parallel-plate cSiAuJFETs independently of channel widths, whereas the dependence is linear for comb-type cSiAuJFETs, which means that electrical tuning of the sensitivity is more effective for the former with respect to the latter. We argue that such a difference between parallel-plate and comb-type sensors is mainly related to slight variation in either thickness or surface area of the cSiAuN layer induced by the different device patterns (e.g. due to corner effects) on the MAE outcomes.

5. Conclusions

Summarizing, in this work, Metal-Assisted Etching (MAE) is successfully demonstrated, for the first time, as a powerful approach for the integration of composite silicon/metal nanostructured materials, specifically composite silicon/gold nanostructures (cSiAuNs), into JFET transistors, for the realization of a novel class of metal-doped silicon-based chemi-transistor gas sensors, namely cSiAuJFET. The cSiAuJFET sensors operate at room temperature and show fast and reliable response to NO_2 in the range 100-500 ppb without significant aging effects up to 48 h of continuous operation, in terms of baseline drift, response times, and sensitivity value, up to two days of continuous operation. Moreover, real-time and effective tuning of the sensitivity of cSiAuJFET sensors by controlling the electrical bias V_{GS} of the transistor gate-terminal is demonstrated and no significant effects of the different V_{GS} voltage values on response times are seen.

Long-term measurements aimed at addressing possible performance degradation of cSiAuJFET sensors beyond 48 h of operation, e.g. due to aging (oxidation) of the porous silicon matrix, and interference measurements aimed at establishing the degree of selectivity of cSiAuJFET sensors, e.g. towards other species (relative humidity) present in the environment, will be subject of future work.

The proposed approach for the fabrication of metal-doped silicon-based chemi-transistor sensors exploiting composite porous silicon/gold materials prepared by metal-assisted etching

also envisages the possibility of tuning the sensor performance by selecting ad-hoc metal catalysts (e.g. Ag, Pt, etc.), thus paving a way towards the CMOS integration of chemi-transistor sensors with improved selectivity, lifetime, and reliability toward specific analytes, as well as improved environmental sustainability. As a consequence, a further outcome is the simultaneous integration on the same silicon chip of chemi-transistors with different metal dopants, that is exploiting different nanostructured silicon/metal composites, and in turn sensing features. This would lead to the development of array of miniaturized sensors with electronically addressable metal-doped silicon nanostructures for E-nose applications. Applications for these small-size, low-power electronic sensor arrays are in detection and identification of toxic/explosive gases for personal safety and air pollution monitoring but also in the chemical and biological sensing field.

6. Experimental Section

Composite porous silicon/gold nanostructures preparation

Composite porous silicon/gold nanostructures are produced both on p^+-type (resistivity of 0.04 Ω cm) and on p-type (resistivity of 2.5–4 Ω cm) CZ-grown, (100)-oriented, silicon substrates by using the MAE of silicon as given in literature.[25, 27] The Si substrates are firstly cleaned to remove organic grease by soaking in acetone (99%, Sigma-Aldrich) and ethanol (99.8%, Fluka Analytical) in ultrasonic bath at room temperature for 10 and 5 min, respectively, then rinsed in de-ionized water two times and blown using dry nitrogen gas. Afterward, the native silicon dioxide is removed by wet etching in a HF (48%, Sigma-Aldrich):ethanol (99.8%, Fluka Analytical) solution (1:1 by vol). Subsequently, Au nanoparticles from 2 mm x 2mm pellets of 99.95% purity gold (Testbourne Ldt.) are deposited by electron beam-assisted thermal evaporation (home-made assembled using Edwards parts) at room temperature and residual pressure of 10^{-5} mbar on top of the cleaned Si substrates. In our experiments different nominal thicknesses of gold, namely 0.7, 1.5 and 3

nm, are deposited at deposition rate of about 3 nm/min. The Si samples coated with gold NPs on top are immersed in an aqueous solution of hydrofluoric acid (HF, 48%, Sigma-Aldrich) and hydrogen peroxide (H_2O_2, 30%, Sigma-Aldrich) for different times (30, 60, 90s) in order to produce the composite porous silicon/gold nansotructures. Each experiment is repeated three times in order to evaluate the average and standard deviation values. The concentrations of HF and H_2O_2 (1:1 by vol.) in the etching solution are chosen according to the literature on this subject so as to enhance reproducibility and uniformity of the resulting nanostructured material.[40] A polytetrafluoroetlyne (PTFE) cell that allows the front-side of the gold-coated samples to be put in contact with the etching solution is used as experimental setup to perform the MAE. When the etching process is over, the samples are rinsed with ethanol (99.8%, Fluka Analytical), then with pentane (99%, Sigma-Aldrich), and eventually dried under nitrogen gas flow for 20 min.

Integration of gold/silicon nanostructures into JFET devices

The cSiAuJFET is fabricated on pn-type silicon wafers (nominal resistivity of p-type and n-type silicon of 0.04 Ω cm and 2-4 Ω cm, respectively). The metallurgical junction between p- and n-type silicon is located at 2.3 μm from the top. A thermal evaporation of 500-nm-thick aluminum film is performed on both p-type silicon (front-side surface) and n-type silicon (back-side surface) under a residual pressure of 10^{-5} mbar. Source and drain contacts (both parallel-plate and comb-finger in shape) are defined (1st mask) on the aluminum film deposited on top of the p-type silicon (front-side surface) by using standard UV photolithography steps: i) positive photoresist (Microposit S1818 G2, Rhom and Haas) spinning at 5000 rpm for 30 s and subsequent pre-baking at 115°C for 75 s on hotplate; ii) UV exposure of the photoresist by using a contact lithography system (MJB3 Karl-Suss mask aligner); iii) photoresist development using a Microposit 351 Developer (Rhom and Haas):H_2O (deionized) 1:5 by volume solution and subsequent post-baking at 115°C for 75 s

on hotplate. Chemical etching of aluminum through the patterned photoresist is performed at room temperature for 5 min in a solution of H_3PO_4 (85%):HNO_3 (65%):CH_3COOH (99.5%):H_2O =16:1:1:2 (by vol). The sample is then rinsed in acetone (99%, Sigma-Aldrich) and ethanol (99.8%, Fluka Analytical) for 15 and 5 min, respectively, in order to fully dissolve the residual photoresist and clean the sample surface. Source and drain aluminum contacts are then protected using a photoresist layer patterned by UV photolitoghraphy (2^{nd} mask) using a magnified replica of the 1^{st} mask that allows the aluminum contacts to be overlapped by photoresist for a width of 50 μm. Electron beam-assisted thermal evaporation of a 1.5 nm-thick gold (pellet, 99.95% purity, Testbourne Ldt.) film is carried out on the front-side surface of the samples, thus enabling deposition of Au nanoparticles on the photoresist-free p-type silicon surface between drain and source contacts.

The selective gold-assisted etching of part of the p-type silicon between drain and source contacts is performed with a HF (48%, Sigma-Aldrich):H_2O_2 (30%, Sigma-Aldrich)=1:1 (by vol) solution for 90 s, so as to integrate the composite porous silicon/gold nanostructured layer on top of the JFET p-channel. A rinse of the sample in acetone (99%, Sigma-Aldrich) and then in ethanol (99.8%, Fluka Analytical) for 15 and 5 min, respectively, is performed to completely remove the photoresist mask covered with gold NPs and clean the sample surface, then the sample is dried under nitrogen gas flow for 20 min.

SEM and XPS analysis

The as-synthesized samples were studied using a scanning electron microscope (SEM) JEOL JSM-6390 at an acceleration voltage of 3kV.

XPS measurements are performed using an Axis ULTRA DLD Spectrometer (Kratos Analytical, UK) with a monochromatic Al K α source operating at 225 W (15kV, 15mA). For each sample a wide-scan spectrum (WS) is acquired in the binding energy range 0-1200 eV with a pass energy of 160 eV and 1 eV step, while high-resolution regions are acquired with a

pass energy of 20 eV and 0.1 eV step. In both cases, the area of analysis is about 700*300 μm^2. The base pressure in the instrument is 10^{-9} mbar. Data analysis and peak fitting is performed by CasaXPS software. Surface charging is corrected considering adventitious C 1s (BE = 285 eV).

Electrical characterization of the chemi-transistors

The sensor characterization under calibrated concentrations of NO_2 in air is carried out using the flow-through technique. The die integrating several cSiAuJFET devices is mounted onto a TO-8 package and placed in a stainless steel test chamber with volume of about 10 cm^3 and temperature controlled with accuracy of ±0.5 °C. For all the experiments, the gas flow-rate in the test chamber is maintained at 200 standard cubic centimeter per minute (sccm), synthetic air (5.0 compressed dry air, Rivoira) is used as carrier gas, NO_2 (1000 ppb in dry air, Rivoira) as target gas, relative humidity is set to zero, and temperature is set to 25 °C. Two digital mass flow controllers (1179B, MKS Instruments) and a digital driving/readout system (PR4000, MKS Instruments) are used to produce synthetic air /NO_2 mixtures with NO_2 concentrations of 0–100-300-500 ppb.

Time-resolved curves (current versus time) of the cSiAuJFETs are measured by biasing the sensors in the saturation region. A Picoammeter/Voltage source (6487, Keithley Instruments), which is used to contemporary set the voltage V_{DS}=-2 V and measure the current I_{DS} between the drain and source terminals over time. A Source-Meter unit (2400, Keithley Instruments) is used to set the voltage V_{GS} at different values, namely 0 V, 0.7 V, 1.5 V, 2.5 V, and simultaneously measure the current I_G between gate (electrical) and source terminals. The cSiAuJFETs are exposed to synthetic air in the test chamber for 60 min prior to measurement in order to settle the output response of the sensor to a stable current value (warm up period). Afterwards the devices are exposed to NO_2 for 30 min (adsorbing phase) and then to synthetic air for 60 min (desorbing phase), repeating the method on the entire NO_2 concentration

window (100-300-500 ppb), whereas the voltage gate is tuned to a new value at the end of each adsorbing phase of 500 ppb.

The measure system is PC-controlled using a LabView interface designed to guarantee the correct timing among of all the different equipments. This comprehends driving the flow controller for setting the right NO_2 concentration and driving the electrical measurement units for recording the current of each cSiAuJFET on the chip.

Figures

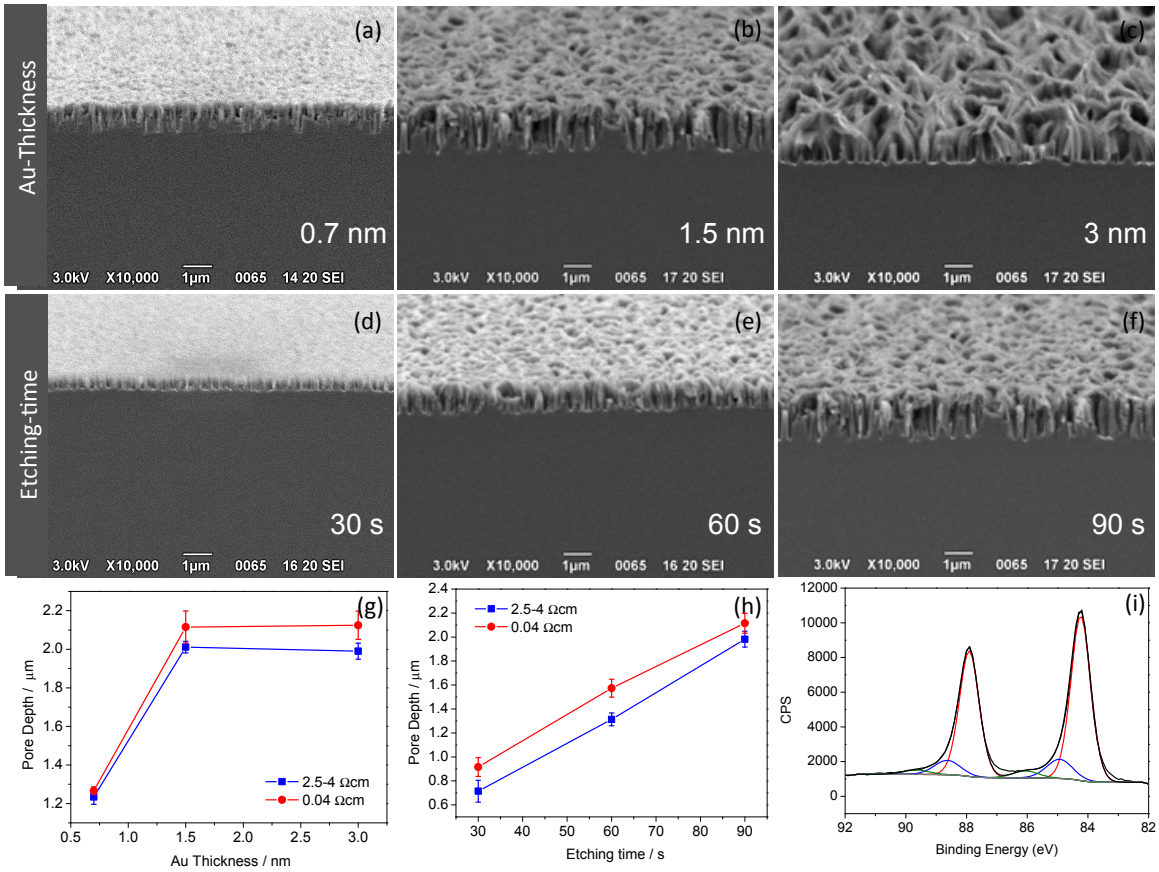

Figure 1. Preparation and characterization of composite porous silicon/gold nanostructures (cSiAuNs) obtained by gold-assisted etching on (100) p-type Si with nominal resistivity of 2.5 Ω cm using HF:H_2O_2:H_2O solution. Cross-sectional scanning electron microscopy (SEM) images of cSiAuNs obtained: with fixed etching time of 90 s and different nominal gold thicknesses (a) 0.7 nm, (b) 1.5 nm, (c) 3 nm; with fixed nominal gold thickness of 1.5 nm and different etching times (d) 30 s, (e) 60 s, (f) 90 s. cSiAuN pore–depth as a function of (g) Au thickness and (h) etching time. (i) X-ray photoelectron spectroscopy (XPS) analysis highlighting Au 4f resolved spectra on cSiAuNs.

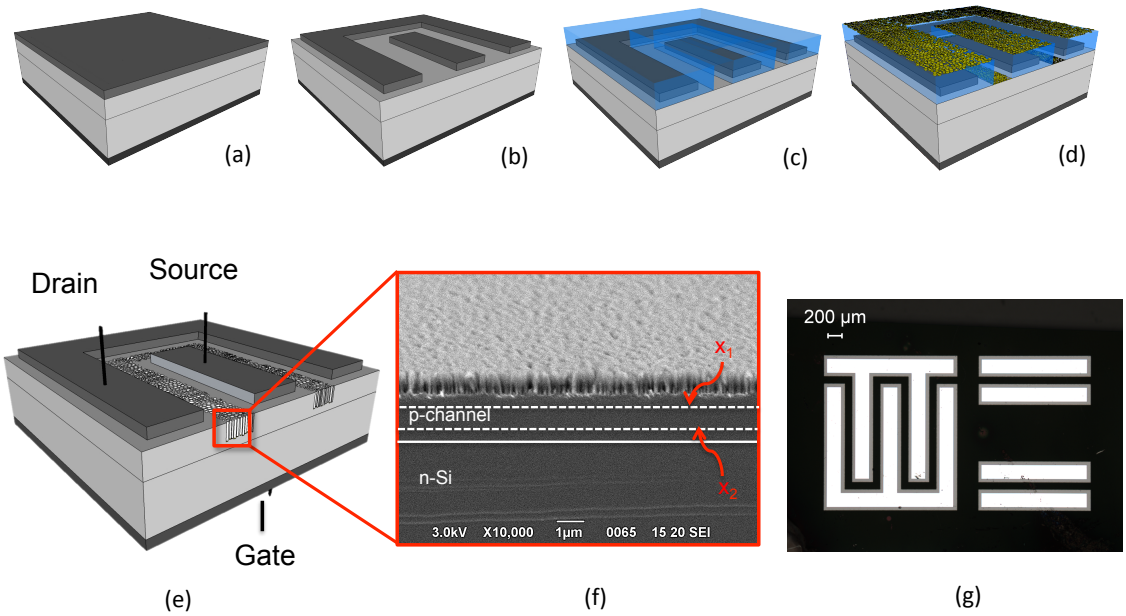

Figure 2. Main fabrication steps of the cSiAuJFET sensor: (a) *p*-*n* silicon wafers (nominal resistivity of *p*-type layer and *n*-type substrate of 0.04 Ω cm and 2-4 Ω cm, respectively, with 500 nm thick Aluminum on both front and back-side surfaces; (b) definition of source (S) and drain (D) terminals of the JFET device by standard photolithography; (c) S and D contacts protection by using a patterned photoresist layer; (d) e-beam thermal evaporation of a 1.5-nm-thick gold layer to obtain gold nanoparticles covering the p-type silicon surface between S and D contacts; (e) synthesis of cSiAuNs between S and D contacts of the JFET device by Au-assisted etching in HF:H_2O_2:H_2O solution. (f) Scanning electron microscopy (SEM) cross-sectional image of the typical cSiAuN selectively integrated between D and S terminals of JFET device, with the depletion regions at the cSiAuN/*p*-channel interface and at the *p*-channel/*n*-silicon interface, x_1 and x_2, respectively, are highlighted. (g) Optical microscope top-view of cSiAuJFET sensors with different S/D configurations: comb-type on the left and parallel-plate on the right.

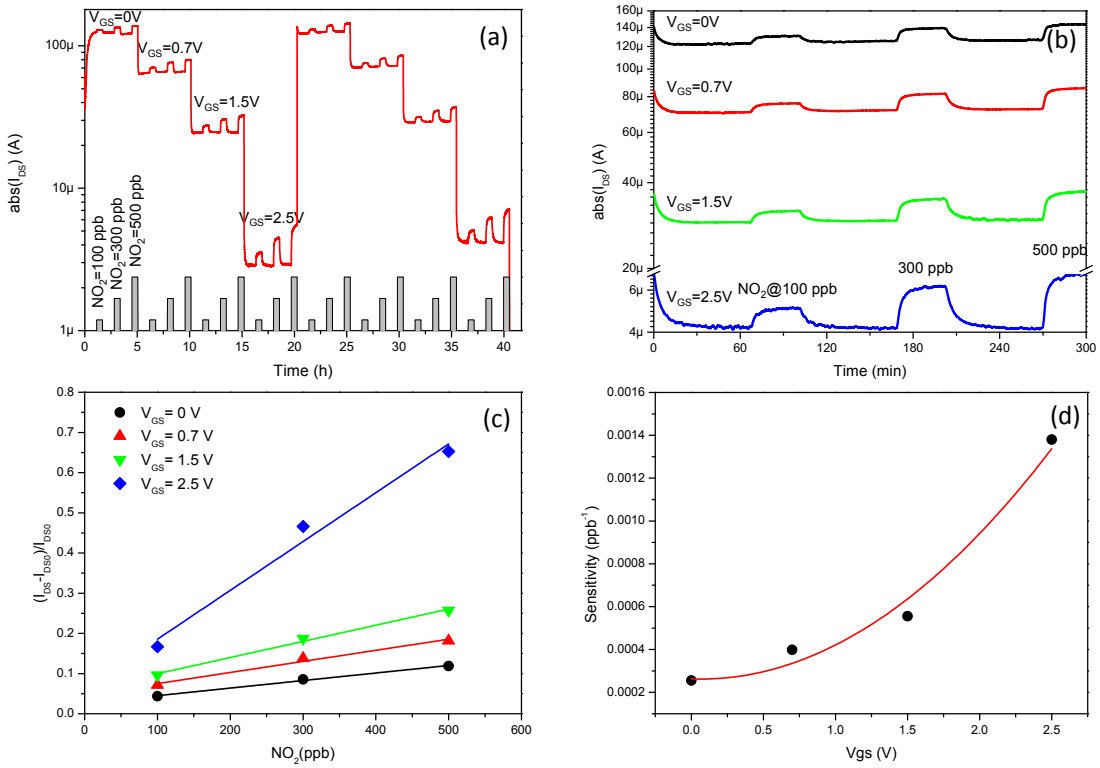

Figure 3 Characterization and performance of parallel-plate cSiAuJFET sensor: (a) Time-resolved curve (current versus time) of cSiAuJFET (parallel-plate D/S configuration) measured upon NO_2 exposure at concentration of 100, 300, 500 ppb for different polarization voltages V_{GS} (from 0 to 2.5 V) up to 48h of continuous operation and (b) in a narrower time-window (1h). (c) Relative current-variation ΔI_R as a function of NO_2 concentration (calibration curve). (d) Experimental sensitivity curve (sensitivity versus gate voltage V_{GS}) and best-fitting of experimental data with a quadratic curve.

Supporting Information

Characterization and performance of comb-type cSiAuJFET sensors and comparison of four cSiAuJFETs integrated on the same silicon die. This information is available free of charge via the Internet at http://pubs.acs.org/

References

1. (EEA), E. E. A., *Europe to Exceed Air Pollutant Emission Limits – NOx in Particular* **2010,** http://www.eea.europa.eu/highlights/europe-to-exceed-air-pollutant (accessed 10, 2014).

2. (NIOSH), T. N. I. f. O. S. a. H., *Documentation for Immediately Dangerous To Life or Health Concentrations (IDLHs)* **2014,** http://www.cdc.gov/niosh/idlh/default.html (accessed 10, 2014).

3. Afzal, A.; Cioffi, N.; Sabbatini, L.; Torsi, L., NOx sensors based on semiconducting metal oxide nanostructures: Progress and perspectives. Sensors and Actuators B: Chemical 2012, 171-172, 25-42.

4. Torsi L.; Dodabalapur A., Organic Thin-Film Transistors as Plastic Analytical Sensors. Analitical Chemistry 2005, 77 (19), 380A-387A.

5. Knopfmacher, O.; Hammock, M. L.; Appleton, A. L.; Schwartz, G.; Mei, J.; Lei, T.; Pei, J.; Bao, Z., Highly stable organic polymer field-effect transistor sensor for selective detection in the marine environment. Nature Communications 2014, 5, 2954.

6. Lee, K.; Ju, B.-K., Carbon-nanotube-based flexible devices using a mechanical transfer method. Physica Status Solidi (a) 2012, 209 (10), 2082-2086.

7. Guo, Y.; Wu, B.; Liu, H.; Ma, Y.; Yang, Y.; Zheng, J.; Yu, G.; Liu, Y., Electrical assembly and reduction of graphene oxide in a single solution step for use in flexible sensors. Advanced Materials 2011, 23 (40), 4626-4630.

8. Lazzerini, G. M.; Strambini, L. M.; Barillaro, G., Addressing reliability and degradation of chemitransistor sensors by electrical tuning of the sensitivity. Scientific Reports 2013, 3, 1161.

9. Zhang, D.; Liu, Z.; Li, T.; Tang, C.; Liu, X.; Han, S.; Lei, B.; Zhou, C., Detection of NO_2 down to ppb Levels Using Individual and Multiple In_2O_3 Nanowire Devices. Nano Letters 2004, 4 (10), 1919-1924.

10. Das, A.; Dost, R.; Richardson, T.; Grell, M.; Morrison, J. J.; Turner, M. L., A Nitrogen Dioxide Sensor Based on an Organic Transistor Constructed from Amorphous Semiconducting Polymers. Advanced Materials 2007, 19 (22), 4018-4023.

11. McAlpine M. C. , A. H., Wang D., Heath J. R. , Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors. Nature Materials 2007, 6, 379-384.

12. Paska, Y.; Stelzner, T.; Christiansen, S.; Haick, H., Enhanced Sensing of Nonpolar Volatile Organic Compounds by Silicon Nanowire Field Effect Transistors. ACS Nano 2011, 5 (7), 5620-5626.

13. Santoro, G.; Yu, S.; Schwartzkopf, M.; Zhang, P.; Vayalil, S. K.; Risch, J. F. H.; Rübhausen, M. A.; Hernández, M.; Domingo, C.; V., R. S., Silver substrates for surface enhanced Raman scattering: Correlation between nanostructure and Raman scattering enhancement. Applied Physics Letters 2014, 104, 243107.

14. Zou, X.; Wang, J.; Liu, X.; Wang, C.; Jiang, Y.; Wang, Y.; Xiao, X.; Ho, J. C.; Li, J.; Jiang, C.; Fang, Y.; Liu, W.; Liao, L., Rational design of sub-parts per million specific gas sensors array based on metal nanoparticles decorated nanowire enhancement-mode transistors. Nano Letters 2013, 13 (7), 3287-3292.

15. Kauffman, D. R.; Star, A., Chemically Induced Potential Barriers at the Carbon Nanotube−Metal Nanoparticle Interface. Nano Letters 2007, 7 (7), 1863-1868.

16. Han, N.; Wang, F.; Hou, J. J.; Yip, S. P.; Lin, H.; Xiu, F.; Fang, M.; Yang, Z.; Shi, X.; Dong, G.; Hung, T. F.; Ho, J. C., Tunable electronic transport properties of metal-cluster-decorated III-V nanowire transistors. Advanced Materials 2013, 25 (32), 4445-4451.

17. Ieva, E.; Bulchholt., K.; Colaianni, L.; Cioffi, N.; Sabbatini, L.; Capitani, G. C.; Lloyd Spetz, A.; Kall, P. O.; Torsi, L., Au Nanoparticles as Gate Material for NOx Field Effect Capacitive Sensors. Sensor Letters 2008, 6 (4), 577-584.

18. Cioffi, N.; Colaianni, L.; Ieva, E.; Pilolli, R.; Ditaranto, N.; Angione, M. D.; Cotrone, S.; Buchholt, K.; Lloyd Spetz, A.; Sabbatini, L.; Torsi, L., Electrosynthesis and characterization of gold nanoparticles for electronic capacitance sensing of pollutants. Electrochimica Acta 2011, 56 (10), 3713-3720.

19. Ahn, J.-H.; Yun, J.; Choi, Y.-K.; Park, I., Palladium nanoparticle decorated silicon nanowire field-effect transistor with side-gates for hydrogen gas detection. Applied Physics Letters 2014, 104, 013508.

20. Peng, K.-Q.; Yan, Y.-J.; Gao, S.-P.; Zhu, J., Synthesis of Large-Area Silicon Nanowire Arrays via Self-Assembling Nanoelectrochemistry. Advanced Materials 2002, 14 (16), 1164-1167.

21. Boarino, L.; Imbraguglio, D.; Enrico, E.; De Leo, N.; Celegato, F.; Tiberto, P.; Pugno, N.; Amato, G., Fabrication of ordered silicon nanopillars and nanowires by self-assembly and metal-assisted etching. Physica Status Solidi (a) 2011, 208 (6), 1412-1416.

22. Peng, K. Q.; Wang, X.; Wu, X. L.; Lee, S. T., Platinum Nanoparticle Decorated Silicon Nanowires for Efficient Solar Energy Conversion. Nano Letters 2009, 9 (11), 3704-3709.

23. Garnett, E. C.; Yang, P., Silicon Nanowire Radial p-n Junction Solar Cells. Journal of American Chemical Society 2008, 130 (29), 9224-9225.

24. Peng, K.-Q.; Wang, X.; Lee, S.-T., Gas sensing properties of single crystalline porous silicon nanowires. Applied Physics Letters 2009, 95, 243112.

25. Li, X., Metal assisted chemical etching for high aspect ratio nanostructures: A review of characteristics and applications in photovoltaics. Current Opinion in Solid State and Materials Science 2012, 16 (2), 71-81.

26. Peng, K.; Wu, Y.; Fang, H.; Zhong, X.; Xu, Y.; Zhu, J., Uniform, axial-orientation alignment of one-dimensional single-crystal silicon nanostructure arrays. Angew Chem Int Ed Engl 2005, 44 (18), 2737-2742.

27. Scheeler, S. P.; Ullrich, S.; Kudera, S.; Pacholski, C., Fabrication of porous silicon by metal-assisted etching using highly ordered gold nanoparticle arrays. Nanoscale Research Letters 2012, 7 (450).

28. Lehmann, H. W.; Frick, K., Optimizing deposition parameters of electron beam evaporated TiO_2 films. Applied Optics 1988, 27 (23), 4920-4924.

29. Zhang, Y.; Franklin, N. W.; Chen, R. J.; Dai, H., Metal coating on suspended carbon nanotubes and its implication to metal-tube interaction. Chemical Physics Letters 2000, 331 (1), 35-41.

30. Dawood, M. K.; Tripathy, S.; Dolmanan, S. B.; Ng, T. H.; Tan, H.; Lam, J., Influence of catalytic gold and silver metal nanoparticles on structural, optical, and vibrational properties of silicon nanowires synthesized by metal-assisted chemical etching. Journal of Applied Physics 2012, 112, 073509.

31. Gaspar, D. P. A. C.; Mateus, T.; Leitao, J. P.; Soares, J.; Falcao, B. P.; Araujo, A.; Vicente, A.; Filonovich, S. A.; Aguas, H.; Martins, R.; Ferreira, I., Influence of the layer thickness in plasmonic gold nanoparticles produced by thermal evaporation. Scientific Reports 2013, 3, 1469.

32. Lehmann, V., *Electrochemistry of Silicon: instrumantation, science, materials and applications* Wiley-VCH, Weinheim, Germany 2002.

33. Huang, Z.; Geyer, N.; Werner, P.; de Boor, J.; Gosele, U., Metal-assisted chemical etching of silicon: a review. Advanced Materials 2011, 23 (2), 285-308.

34. Chern, W.; Hsu, K.; Chun, I. S.; Azeredo, B. P.; Ahmed, N.; Kim, K. H.; Zuo, J. M.; Fang, N.; Ferreira, P.; Li, X., Nonlithographic patterning and metal-assisted chemical etching

for manufacturing of tunable light-emitting silicon nanowire arrays. Nano Letters 2010, 10 (5), 1582-1588.

35. Tsakalakos, L.; Balch, J.; Fronheiser, J.; Korevaar, B. A.; Sulima, O.; Rand, J., Silicon nanowire solar cells. Applied Physics Letters 2007, 91, 233117.

36. Peng, K. Q.; Hu, J. J.; Yan, Y. J.; Wu, Y.; Fang, H.; Xu, Y.; Lee, S. T.; Zhu, J., Fabrication of Single-Crystalline Silicon Nanowires by Scratching a Silicon Surface with Catalytic Metal Particles. Advanced Functional Materials 2006, 16 (3), 387-394.

37. Cruz, S.; Hönig-d'Orville, A.; Müller, J., Fabrication and Optimization of Porous Silicon Substrates for Diffusion Membrane Applications. Journal of The Electrochemical Society 2005, 152 (6), C418-C424.

38. Peng, K.; Lu, A.; Zhang, R.; Lee, S.-T., Motility of Metal Nanoparticles in Silicon and Induced Anisotropic Silicon Etching. Advanced Functional Materials 2008, 18 (19), 3026-3035.

39. Laminack, W. I.; Gole, J. L., Light Enhanced Electron Transduction and Amplified Sensing at a Nanostructure Modified Semiconductor Interface. Advanced Functional Materials 2013, 23 (47), 5916-5924.

40. Oh, Y.; Choi, C.; Hong, D.; Kong, S. D.; Jin, S., Magnetically guided nano-micro shaping and slicing of silicon. Nano Letters 2012, 12 (4), 2045-2050.

41. Patolsky, F.; Zheng, G.; Lieber, C. M., Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species. Nature Protocols 2006, 1 (4), 1711-1724.

42. Zhao, L.; Siu, A. C.-L.; Petrus, J.A.; He, Z.; Leung, K.T., Interfacial Bonding of Gold Nanoparticles on a H-terminated Si(100) Substrate Obtained by Electro- and Electroless Deposition. Journal of American Chemical Society 2007, 129 (17), 5730-5734.

43. Fabre, B.; Hennous, L.; Ababou-Girard, S.; Meriadec, C., Electroless patterned assembly of metal nanoparticles on hydrogen-terminated silicon surfaces for applications in photoelectrocatalysis. ACS Appl Mater Interfaces 2013, 5 (2), 338-343.

44. Sundaravel, B. S. K.; Kuri, G.; Satyam, P. V.; Dev, B. N.; Bera, S.; Narasimhan, S. V. ; Chakraborty, P.; Caccavale, F., XPS and SIMS analysis of gold silicide grown on a bromine passivated Si(111) substrate. Applied Surface Science 1999, 137 (1-4), 103-112.

45. Sayed, S.Y.; Wang, F.; Malac, M.; Meldrum, A.; Egerton, R. F.; Buriak, J. M. , Heteroepitaxial Growth of Gold Nanostructures on Silicon by Galvanic Displacement. ACS Nano 2009, 3 (9), 2809-2817.

46. Forleo, A.; Francioso, L.; Capone, S.; Siciliano, P.; Lommens, P.; Hens, Z., Synthesis and gas sensing properties of ZnO quantum dots. Sensors and Actuators B: Chemical 2010, 146 (1), 111-115.

47. Boarino, L.; Geobaldo, F.; Borini, S.; Rossi, A.; Rivolo, P.; Rocchia, M.; Garrone, E.; Amato, G., Local environment of Boron impurities in porous silicon and their interaction with NO_2 molecules. Physical Review B 2001, 64, 205308.

48. Timoshenko, V.; Dittrich, T.; Lysenko, V.; Lisachenko, M.; Koch, F., Free charge carriers in mesoporous silicon. Physical Review B 2001, 64, 085314.

49. Barillaro, G.; Lazzerini, G. M.; Strambini, L. M., Modeling of porous silicon junction field effect transistor gas sensors: Insight into NO_2 interaction. Applied Physics Letters 2010, 96, 162105.

50. Borini, S.; Boarino, L.; Amato, G., Slow conductivity relaxation and simple aging in nanostructured mesoporous silicon at room temperature. Physical Review B 2007, 75, 165205.

51. Zhang, Y.; Kolmakov, A.; Chretien, S.; Metiu, H.; Moskovits, M., Control of Catalytic Reactions at the Surface of a Metal Oxide Nanowire by Manipulating Electron Density Inside It. Nano Letters 2004, 4 (3), 403-407.

52. Mubeen, S.; Moskovits, M., Gate-tunable surface processes on a single-nanowire field-effect transistor. Advanced Materials 2011, 23 (20), 2306-2312.

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