mm-wave integrated wireless transceiver: enabling technology for high bandwidth short-range networking in cyber physical systems

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Abstract

Emerging application scenarios for Cyber Physical Systems often require the networking of sensing and actuation nodes at high data rate and through wireless links. Lot of surveillance and control systems adopt as input sensors distributed video cameras operating at different spectral ranges and covering different fields of view. Arrays of radio/light detection and ranging (Radar/Lidar) sensors are often used to detect the presence of targets, of their speeds, distance and direction. The relevant bandwidth requirement amounts to some Gbps. The wireless connection is essential for easy and flexible deployment of the sensing/actuation nodes. A key technology to keep low the size and weight of the nodes is the fully integration at mm-waves of wireless transceivers sustaining Gbps data rate. To this aim, this paper presents the design of 60 GHz transceiver key blocks (Low Noise Amplifier, Power Amplifier, Antenna) to ensure connection distances up to 10 m and data rate of several Gbps. Around 60 GHz there are freely-available (unlicensed) worldwide several GHz of bandwidth. By using a CMOS Silicon-on-Insulator technology RF, analog and digital baseband circuitry can be integrated single-chip minimizing noise coupling. At mm-wave the wavelength is few mm and hence even the antenna is integrated on chip reducing cost and size vs. off-chip antenna solutions. The proposed transceiver enables at physical layer the implementation in compact nodes of links with data rates of several Gbps and up to 10 m distance; this is suited for home/office scenarios, or on-board vehicles (cars, trains, ships, airplanes) or body area networks for healthcare and wellness.

Introduction

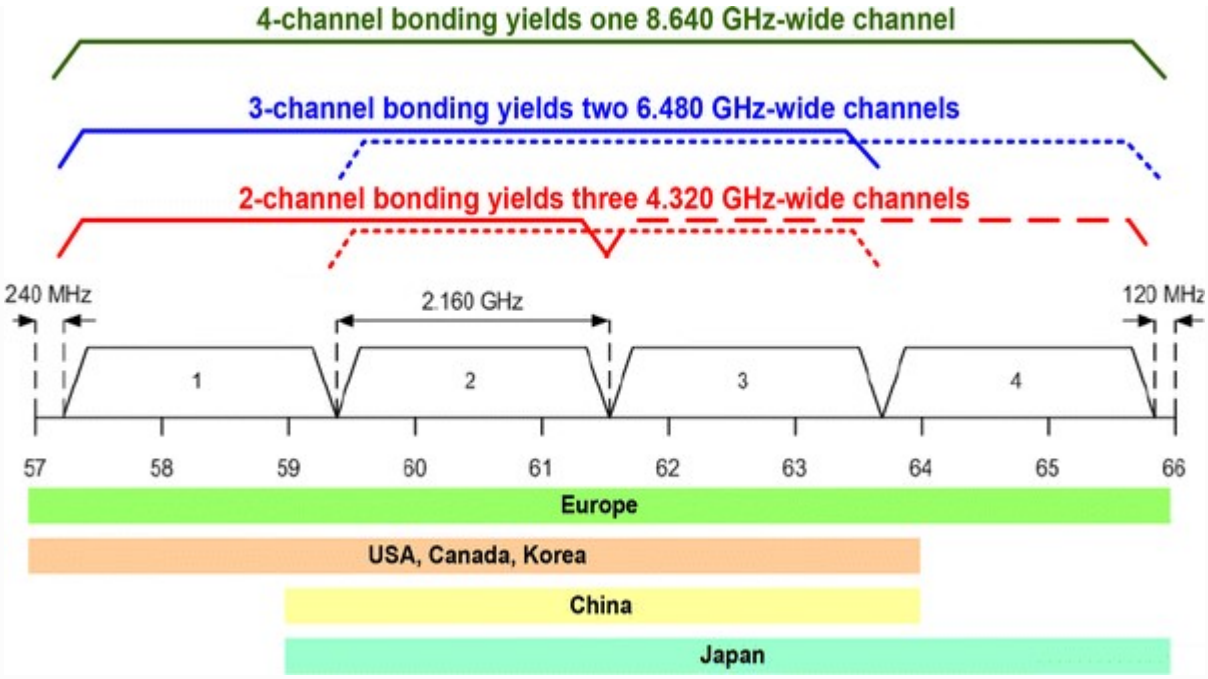
Most of today control or computing systems follow a distributed paradigm to improve the scalability and flexibility of the solution, to increase the interoperability of subsystems from different providers/vendors and to reduce the “single point of failure” risk of a centralized approach. Particularly, CPS are complex feedback systems characterized by the connection at increasing data rates of all the nodes belonging to the network:

sensors, actuators, processing or control units, storage units, diagnostic access points, machine-to-machine (M2M) or human-to-machine (HMI) interfaces. For CPS applications heterogeneous connection technologies may be used (copper pair, coax-cable, fiber and wireless at sub-GHz, microwave or mm-wave frequencies) with wide-, local- or short- area networking. In this scenario there is a growing use of high speed sensors (arrays of photo and video cameras, thermo-cameras, LIDAR, RADAR,…to name just a few) and of high speed accesses from the nodes to a centralized cloud in charge of data processing, storage and system control. High bandwidth connections are also required to meet the stringent requirements (low latency, high data throughput) of real-time M2M and HMI interfacing. This approach increases the need for high-speed links, with wireless connections to avoid wiring harness, beyond 1 Gbps (Lee 2010; Sheng et al. 2013; Fang-Jing et al. 2011; Wean et al. 2013; Lu 2014; Lumpkins 2014; Andrews et al. 2014; Saponara et al. 2015; Tsukizawa 2013; Vaughan 2010). Hence, at the physical level of a CPS there is the need of high-speed wireless solutions reaching data rates well beyond the tens of Mbps offered today by Wireless LAN or Bluetooth technologies. Other key aspects for the widespread diffusion of WSAN, and more in general of CPS, are (1) the worldwide availability of the spectrum for free (unlicensed) to keep low operating costs; (2) the integration of the hardware towards single-chip solutions to keep low the size and weight of the nodes.

To this aim, some standardization initiatives such as the Wi-Gig or WirelessHD alliances have been already started and new standards are emerging such as the IEEE 802.11ad or the ECMA-387 (standardized also as ISO/IEC 13156) (Andrews et al. 2014; Saponara et al. 2015; Tsukizawa 2013; Vaughan 2010). Gbps wireless data transfer is also the target of the upcoming 5G generation of mobile communications (Andrews et al. 2014). Since Fiber to the Cabinet/Home (FTTC/FFTH) solutions are already available for high speed cabled connections, the next challenge to win is the development of Gbps wireless connections (Lumpkins 2014; Andrews et al. 2014; Saponara et al. 2015; Tsukizawa 2013; Vaughan 2010). This trend characterizes application fields such as transports, surveillance, domotics, health at home, aerospace, defence, smart cities and smart offices.

To address the above issues the paper proposes the design of integrated transceivers, operating at mm-waves around 60 GHz, able to reach a transfer data rate of several Gbps at 10 m. At such frequencies, see Fig. 1, there is worldwide available a free spectrum of several GHz with different channelization options: multiple channels with bandwidth higher than 2 GHz up to a single channel of about 9 GHz from 57 to 66 GHz.

Fig. 1



Worldwide freely-available spectrum for high-speed WSAN and CPS and example channelization in ECMA-387

Differently from traditional solutions where mm-wave devices are realized through expensive dedicated technologies (HBT-Heterojunction Bipolar Transistors or HEMT-High Electron Mobility Transistors in GaAs, InP or other III-V technologies) this paper proposes the design of the key blocks of the mm-wave transceiver using the same CMOS technology of the digital part. This can enable the diffusion of local area network of high-speed sensing, actuation and processing nodes in home and office scenarios, or on-board vehicles such as cars, trains, satellites, ships, airplanes. Indeed is the RF part the most challenging to be designed while the state of art is rich of solutions for ADC and baseband signal processing (Saponara et al. 2009; Fanucci et al. 2001). Hereafter Sect. 2 presents the 60 GHz transceiver architecture. Sections 3, 4 and 5 discuss the design of key blocks such as low noise amplifier (LNA), integrated antenna and power amplifier (PA). Section 6 presents performance results for the whole transceiver. Section 7 draws some conclusions and discusses adherence of the proposed work to standards such as ECMA-387 (ISO/IEC 13156).

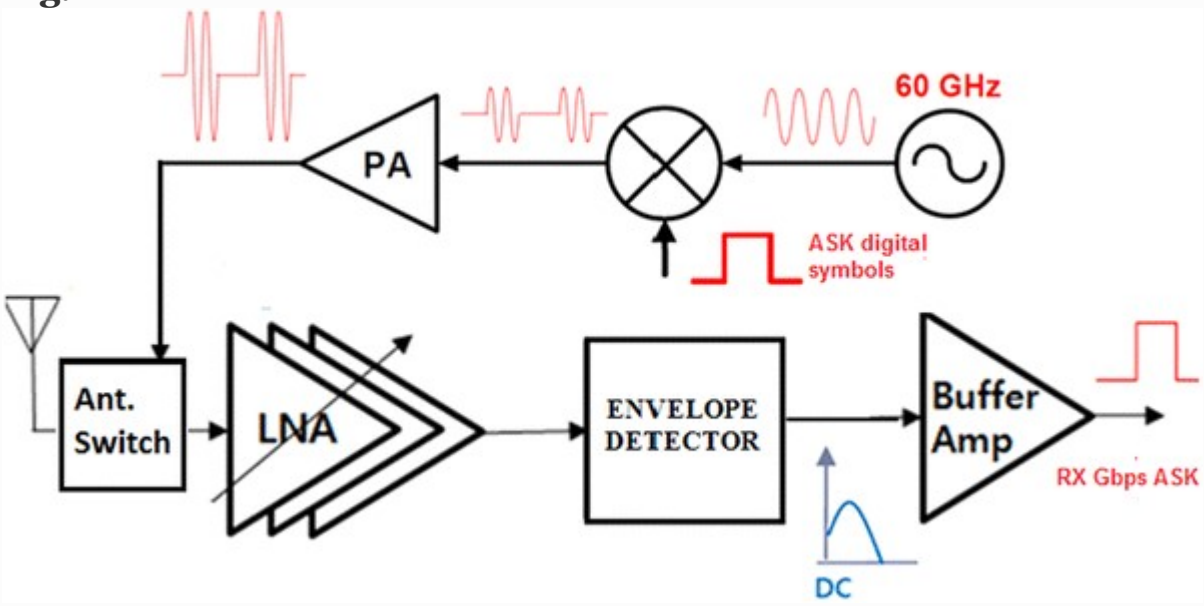
60 GHz transceiver architecture and key blocks specifications

Transceiver architecture

Due to the peak of absorption of oxygen around 60 GHz, the attenuation of electromagnetic waves makes this frequency range suitable mainly for short-range scenarios up to 10 m. At 60 GHz the wavelength amounts to few

millimeter and also the antenna can be integrated on chip further reducing area and complexity. In the transceiver architecture of Fig. 2 we adopt a simple modulation scheme like the in-coherent ASK (amplitude shift keying) to keep small the complexity and cost of the transceiver. Even with the ASK spectrum efficiency of 1 bit/s/Hz a data rate of several Gbps can be achieved, thanks to the availability of channels with a spectrum of several GHz (see Fig. 1). As reported in Fig. 2 for an in-coherent ASK just an envelope detector is needed at receiver side. Avoiding complex PLL (phased locked loop) for local oscillators and synchronizations and avoiding high-Q LC filter the whole transceiver can be integrated single-chip with a small area and with very low power consumption in wireless sensing or actuation nodes. Adopting complex Orthogonal Frequency Division (OFDM) systems, with Quadrature and Amplitude modulations, the data rate can growth up to tens of Gbps. For both transceiver architectures, incoherent ASK and multicarrier OFDM, the key blocks are the LNA at receiver side, the PA at transmitter side and the integrated antenna. To be noted that at transmitter side, by using as ASK coefficients values with the same amplitude and opposite signs, we can realize also a BPSK (binary phase shift keying) modulator. It is worth noting that in this work, differently from similar other mm-wave transceiver architectures (Saponara et al. 2014, 2015) where two antennas are implemented, the same antenna is used for both the receiver (RX) and the transmitter (TX). To this purpose, the transceiver implemented in this work adopts a time-division duplexing scheme and a voltage-controlled antenna switch. The antenna switch is realized following the approach patented in Geddada et al. (2014).

Fig. 2



Architecture of ASK transceiver for low-complex mm-wave wireless networking with shared TX/RX antenna

All the key blocks (LNA, antenna and PA) have been designed in 65 nm CMOS Silicon On Insulator (SOI) technology from STMicroelectronics with a voltage supply of 1.2 V, 6 copper-staked layers (M_1–M_{6Z}) and an aluminum capping layer. The SOI version of the CMOS technology allows for much better performance of the RF circuitry vs. classic CMOS bulk technology due to its higher resistivity substrate (1 kΩ cm instead of standard 20 Ω cm). Parasitic passive components and RF power irradiation losses in the substrate are minimized still avoiding the high extra costs of hetero-junction technologies traditionally used for mm-wave circuits such as SiGe HBT, GaAs or InP HEMT. The 65 nm CMOS SOI technology node is also a low cost solution when compared to cutting edge silicon technologies, such as the 14-nm Fin-FET used for multi-processor systems-on-chip. Thanks to the insulator substrate in CMOS SOI the signal coupling between the digital, RF, and baseband analog parts of the circuit is reduced. Summarizing, CMOS SOI technology provides the right trade-off between performance and cost for the mixed-signal electronics required in CPS nodes.

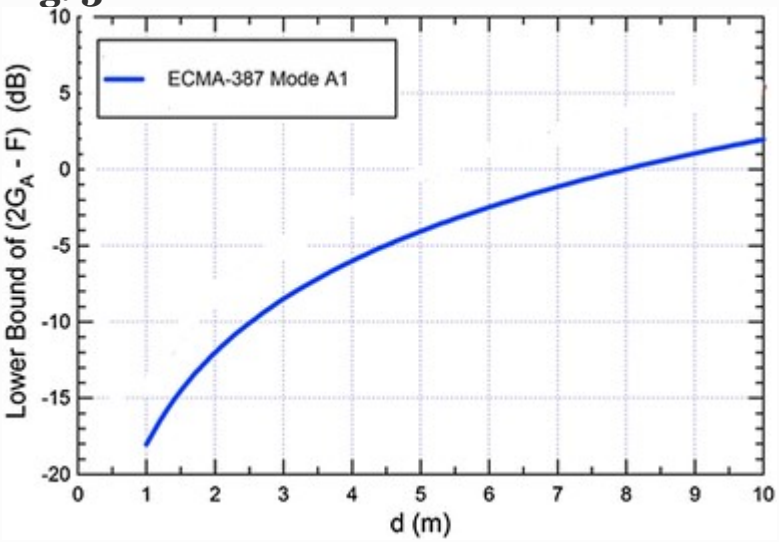
System-level model for specifications of key blocks

A system-level model of a whole 60 GHz link considering the transceiver architecture of Sect. 2.1 has been built in Matlab Simulink environment. To this aim the specifications of the ECMA-387 standard, mode A1, have been considered as reference. ECMA-387, standardized also as ISO/IEC 13156, foresees different configuration with both single-carrier (mandatory) and OFDM (optional) transmission schemes. Supported modulations include basic solutions such as ASK, OOK and BPSK or more complex ones for higher bit-rates such as QPSK, NS8QAM, 16QAM. At physical layer the whole bandwidth from 57 to 66 GHz can be used and is divided in 4 channels, each of 2.16 GHz, that can be bonded to form wider channels up to 8.64 GHz.

Using this system-level model the specifications of the key blocks of the transceiver (LNA, antenna and PA) have been derived. As an example of the possible outputs of the system-level model, Fig. 3 shows the dependence of the link distance *d* on both the receiver noise figure F and the antenna gain G_A. In Fig. 3 we considered for the ECMA-387 mode A1 standard a packet error rate (PER) below 8 % with packets of 1 kB, convolutional Reed-Solomon coding, 4 Gbps target data-rate. From Fig. 3, to achieve a lower bound of ($2G_A$-F) > 1 dB to reach a link distance of 10 m, the antenna gain G_A should be at least 3 dBi while the noise figure (F) of the receiver should not exceed 5 dB over the whole 57–66 GHz spectrum. 60 GHz mixers in 65 nm CMOS SOI are already available in literature with a noise figure below 13 dB (Chong 2014). Therefore, according to the Friis' formula, if we are able to design an LNA with a gain of at least 15 dB then its noise figure, NF, will determine the noise figure F of the whole receiving chain. For the PA a linear circuit should be designed, able to reach a 1 dB output compression point

(OP1 dB) of 10 dBm. The linearity of the PA is important in non-constant envelope schemes, such as ASK or OFDM (which is characterized by high peak to average power ratio) considered in this work. As proved by simulations in Tubbax et al. (2001) with an OFDM communication system an increase in 0.5 dB of the PA non linearity leads to a BER (bit error rate) increase of one order of magnitude.

Fig. 3



System-level simulation of an ECMA-387 link, dependence of the link distance *d* with antenna gain G_A and receiver noise figure *F*

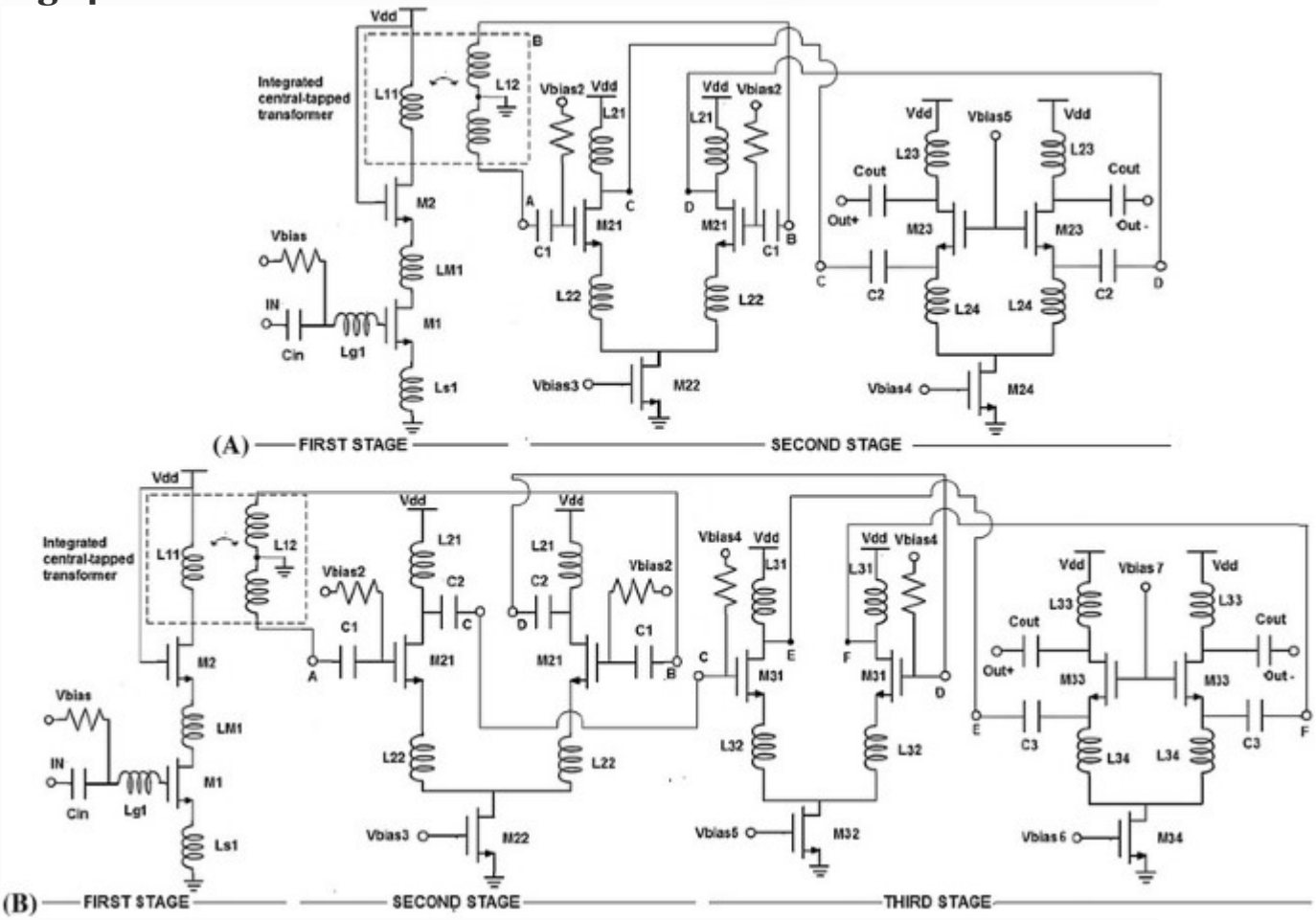
Wideband LNA circuit design

To reach the LNA specifications of NF <5 dB, gain >15 dB from 57 to 66 GHz, we designed 2-stage and 3-stage LNAs with inter-stage LC-matching in 65 nm CMOS SOI.

3D electromagnetic characterizations of active/passive circuits and layout-level silicon design have been carried out in HFSS and Cadence CAD environments respectively. The relevant circuitry at transistor level are shown in Fig. 4. Differently from state-of-art LNA designs with pre-defined 50 Ω input matching constraint, in this work, co-designing on-chip also the antenna, the impedance matching is a new degree of freedom to be tuned during the design phase to optimize circuit performance. Indeed Voinigescu et al. (2007), for 60 GHz applications, suggests the following design metrics to define the transistor width of the first LNA stage in order to minimize the noise figure: a Jopt = 0.15 mA/μm current density and an Rs_{opt} = 1200 μm Ω source impedance. However, if the final LNA input impedance is constrained to a predefined value of 50 Ω, the above rules lead to a fixed transistor width of about 24 μm and to a fixed current value of 3.6 mA. Other works in literature (Baki 2006) proved that, while keeping the Jopt and Rs_{opt} values in

Voinigescu et al. (2007) to minimize the noise figure, to optimize also the linearity and gain performance of the amplifier the transistor width should be larger than those in Voinigescu et al. (2007), i.e. the input impedance should be different from 50 Ω. In our design we fixed the MOSFET current density close to 0.15 mA/μm (for all stages) and then different configurations of the LNA parameters were simulated allowing for different LNA input impedance values and different gain and noise figure trade-offs. To limit the design space to be explored the input impedance should be in a range from few Ω to 100 Ω. For this range an on-chip antenna with matched source impedance can be easily designed. The gain and NF with matched LNA-antenna impedance should be higher than 15 dB and lower than 5 dB, respectively, over the whole 57–66 GHz band.

Fig. 4



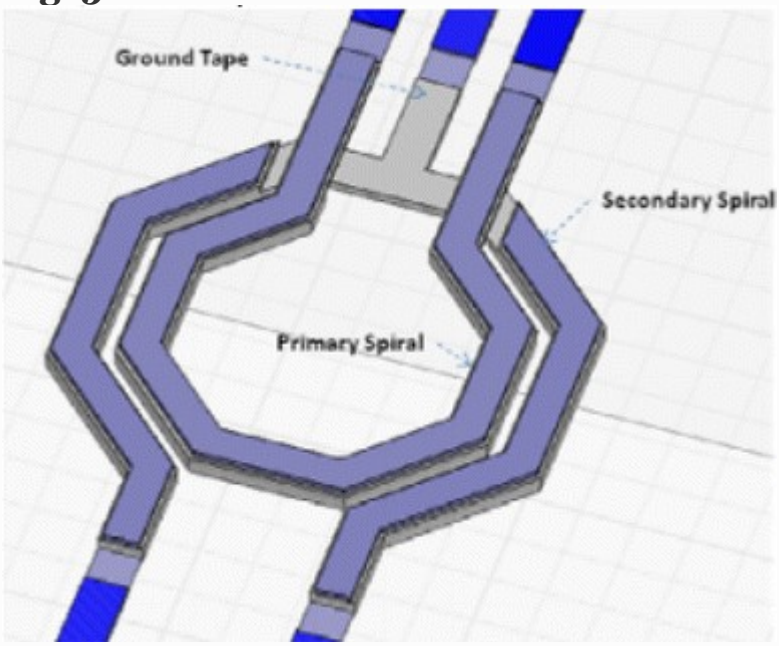
a Building circuitry of 2-stage LNA; **b** building circuitry of 3-stage LNA

The proposed 2-stage LNA is composed by a single-ended cascode stage (First Stage in Fig. 4a) which provides a differential output to a fully differential second stage of amplification through an integrated inter-stage transformer that provides, in addition, the maximum power delivery from

the first to the second stage of the LNA. The Second Stage is a fully differential cascode amplifier, modified vs. conventional solutions to remove the staked transistor, common-source (CS) and common-gate (CG) and thus reducing the problems due to low-supply voltage in scaled technologies.

The inter-stage transformer, see its layout in Fig. 5, consists of two octagonal and symmetrical coupled planar inductors, both with 24 μm of diameter, one turns each, 3 μm spaced and 6 μm wide. The structure has been designed by using all the metal layers available in the technology: thick copper-staked layers (M_1–M_{6Z}) and aluminum capping layer (AP). Near to the intersection the first spiral has been designed in M_{6Z} and AP, whereas the secondary spiral in M_1–M_5. This structure does not need under-passes, so eliminating the series parasitic effects. In the CMOS SOI implemented versions the primary spiral exhibits a self-inductance (LTP) of 183 pH with an associated quality factor (QTP) equal to 15.5, whereas the secondary spiral exhibits the same self-inductance (LTS = 147 pH) with a QTS equal approximately to 30, at 60 GHz. The W (width) parameter of the M1 and M2 MOS of the First Stage has been set to 40 μm, with transistors polarized at weak inversion (VGS of roughly 0.8 V).

Fig. 5



Layout of the inter-stage transformer

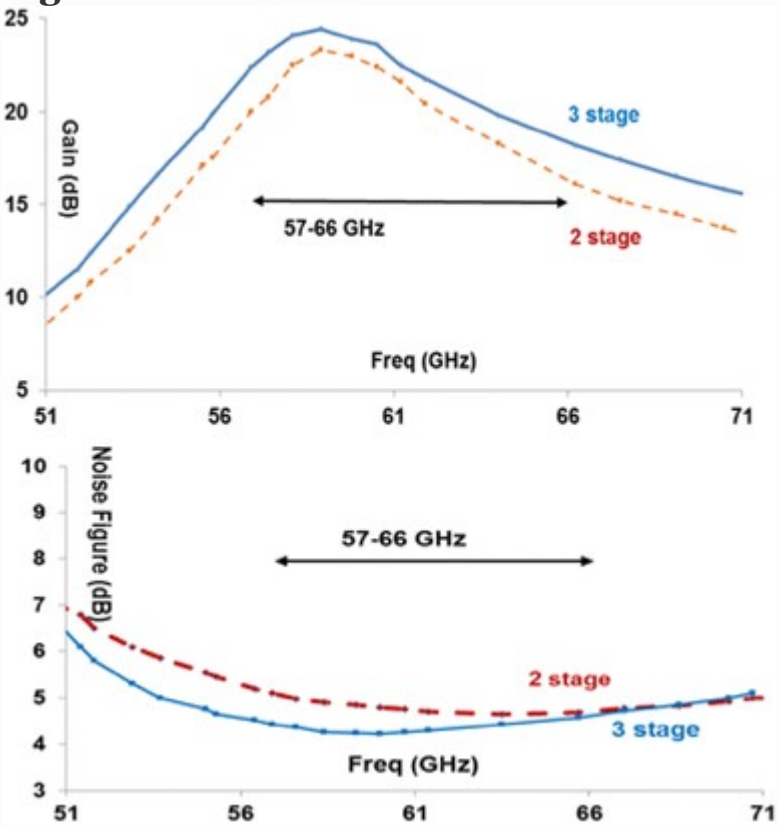
The functioning of all circuits proposed in the paper have been verified during design phase for all corner cases (worst, typical, best) taking into count PVT (process-voltage-temperature) variability.

The size of the transistors in other stages is from 30 μm to 60 μm, while the value of L (channel length) has been taken at its minimum, 0.06 μm. The second stage in Fig. 4a is a fully differential cascode, which allows the increase of the power gain and the benefits of the common mode rejection ratio (CMRR). Indeed in all parameter and technology configurations considered in this work the First Stage alone allows for a gain below 10 dB, much lower than the minimum 15 dB target. The cascode configuration is implemented by using a common-source and an AC coupled common-gate stage instead of the standard configuration like that realized for the first single-ended stage. In this way also in the Second Stage, as in the input one, there are only two staked transistors between voltage supply, V_{DD} = 1.2 V, and ground.

To further increase LNA gain performance, although at increased power consumption, a 3-stage LNA configuration has been also designed. In the 3-stage LNA the first and third stages in Fig. 4b are de-facto similar to the already discussed First and second stages of Fig. 4a. A new intermediate stage is added in the 3-stage LNA (second stage in Fig. 4b) consisting of a differential common source amplifier AC coupled with the preceding and following stages.

As shown in Fig. 6, the 2-stage LNA circuit in CMOS SOI technology has a power gain higher than 15 dB (peak value 23.3 dB at 59 GHz) and a noise figure lower than 5 dB over the 57–66 GHz spectrum. Such values refer to a 30 Ω source impedance [respecting the above-mentioned Rs_{opt} rule derived from Voinigescu et al. (2007)] that during the design tuning has been found as a value ensuring a good trade-off between noise, gain and bandwidth. The 30 Ω matching impedance has been easily achieved when designing the integrated antenna in Sect. 4. The power consumption of the 2-stage LNA at 1.2 V supply is about 26 mW. The contribution of the first stage alone is about 7 mW but this solution does not meet the required gain performance. The 3-stage LNA in CMOS SOI technology gets the target performance (noise figure below 5 dB) over the 57–66 GHz spectrum with a power gain increased vs. the 2-stage version in the same technology (see Fig. 6): peak gain of 24.4 dB at 58.9 GHz and a gain of at least 18 dB from 57 to 66 GHz. The performance improvement (+1.1 dB peak gain, −0.5 dB NF) of the 3-stage LNA vs. the 2-stage circuit is paid in terms of power consumption increase of 30 % (35 mW instead of 26 mW). The input return loss (S_{11} parameter) for 2- and 3-stage LNAs is below −10 dB for the 57–66 GHz band. The stability factor (K) of both 2- and 3-stage LNAs in SOI CMOS technology are always greater than 4, demonstrating that the designed LNAs are unconditionally stable at 60 GHz. We also checked the BIBO (bounded input bounded output) stability of 2- and 3-stage LNAs by analyzing in time-domain the transient response to impulse inputs.

Fig. 6

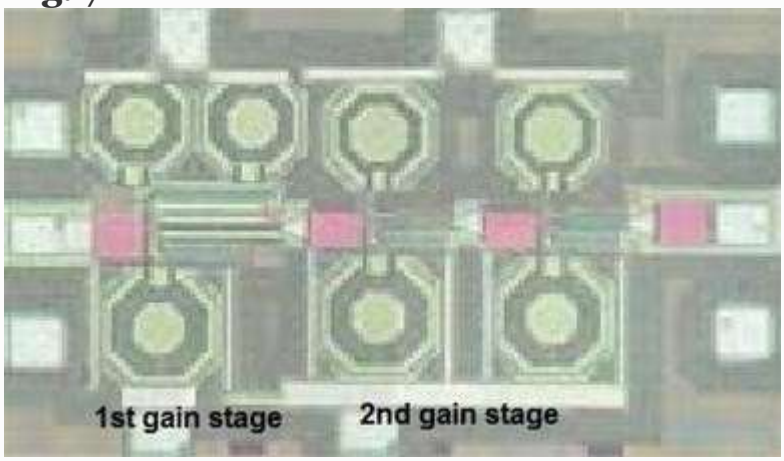


Gain and noise figure for 2- and 3-stage LNAs

Summarizing the single-stage, 2-stage and 3-stage LNAs in CMSO SOI have been designed: keeping as targets a maximum NF of 5 dB and a minimum gain of 15 dB the best solution is the 2-stage LNA that meets the above constraints with a minimum power cost of about 26 mW.

Figure 7 shows the 2-stage LNA chip. Table 1 compares the achieved performance vs. recent LNA designs in 65 nm CMOS technology node (Saponara et al. 2014; Weyers et al. 2008; Martineau et al. 2008; Siligaris et al. 2011). To be noted that our design has been optimized to cover a wide bandwidth range of 9 GHz from 57 to 66 GHz (and hence we report in Table 1 minimum and maximum gain) while other state-of-art designs are often optimized in terms of gain and NF around a smaller band, typically 2–3 GHz around 60 GHz.

Fig. 7



2-Stage LNA chip

Table 1 LNA results in 65 nm CMOS tech. and comparison with state-of-art

Wideband on-chip antenna design

For the antenna design, we explored in 65 nm CMOS technology four different topologies allowing for different trade-offs between gain, bandwidth and area: dipole, inverted-F and bow-tie plus a double-slot from Saponara (2012) as a comparison.

The half-wave dipole antenna in CMOS SOI technology has been realized using the M_{6Z} metal layer and has a length of 760 μm; the width of the two-dipole arms is 22.76 μm with a gap between them of 1.1 μm. The integrated dipole can be connected to the active circuitry with a coplanar strip-line of 334 μm length. Such values have been sized to meet the impedance matching of the LNA designed in Sect. 3 and to maximize the gain around 60 GHz.

Table 2 shows the area occupied when placing a rectangular macrocell including the antenna in the chip layout. The real area occupation should consider also that other active or passive circuits should not be placed in the near reactive-field region of the radiating structure. This imposes a distance from the antenna structure of at least $\lambda/2\pi$, about 400 μm in our case. At layout level an area of about 1.7 mm^2 should be reserved to the dipole antenna. The same antenna designed in CMOS bulk technology has similar area (the length and width sizing depends mainly on the operating wavelength) while the losses due to the low resistivity substrate lead to worse performance in bulk CMOS.

Table 2 On-chip antenna results in 65 nm CMOS tech. and comparison with state-of-art

To reduce the antenna area occupation we considered also a folded PIFA (planar inverted F antenna): fundamentally, it is a folded quarter-wave monopole with a ground plane and can be realized with lower area occupation than dipole and double slot topologies in a 450 × 250 μm^2 box (0.1125 mm^2). A 1250 × 1050 μm^2 (1.3 mm^2) space has to be left without integrated active or passive devices. The achieved gain is roughly 6 dB lower than the half-wave dipole with a poor radiation efficiency and a return loss bandwidth limited to 5 GHz. Hence, the PIFA area saving of roughly 25 % vs. the dipole antenna topology does not justify its adoption for WSAN due to the reduction in bandwidth and gain.

A planar bow-tie dipole has been also considered since it is a topology known to provide ultra wide band radiation performance. The bandwidth and the lower frequency of this kind of antenna mainly depend on the length of the arms, the center angle, and the length of the smaller base of the trapezium that defines the radiating structure. In this work the bow-tie antenna has been designed with 337 μm length for the arm, 18 degrees for the center angle and 75.5 μm for the length of the smaller base of the trapezium. The bow-tie antenna can be connected to the LNA through a stripline of length 648 μm. The bow-tie allows for the best bandwidth performance since the S_{11} is below −10 dB for more than 20 GHz starting from a 50 GHz lower limit. However, its gain is far from the system-level requirements.

As an alternative to the above antennas, we evaluated also the double slot topology proposed in Siligaris et al. (2011) with a coplanar wave guide feeding line of length 560 μm and width 22 μm. The double slot has a length of 910 μm and a width of 22.76 μm. The gap between antenna and ground plane is 40 μm. This antenna has good radiation efficiency, 67 %, and maximum gain result, 4.44 dBi, among the antenna topologies considered in this work. The peak return loss (S_{11}) has also a good value, −23 dB. However, the useful bandwidth of the double slot antenna, where the S_{11} is below −10 dB, is only from 59 to 60 GHz. The result of 1 GHz useful bandwidth is too narrow with respect to the target spectrum of interest from 57 to 66 GHz.

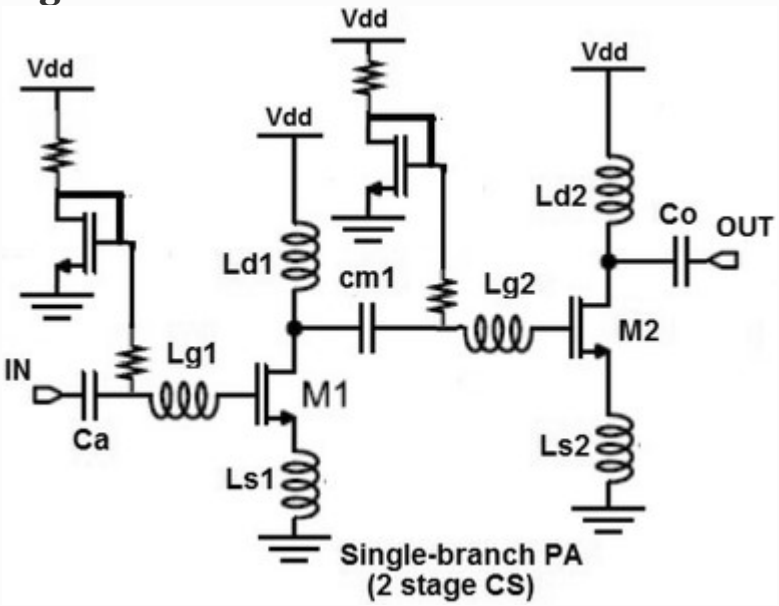
As conclusions, considering the trade-off among multiple design parameters (gain, efficiency, useful bandwidth, area occupation) a dipole topology has been selected and implemented in 65 nm SOI technology (first row of Table 2).

Linear power amplifier

As discussed in Sect. 2.2 the linearity of the PA is important in non–constant envelope schemes, such as the ASK or the OFDM considered in this work. To this aim, more efficient but non linear topologies such as class-C or class-E RF PA have been avoided, and a class-A amplifier has been designed. The

proposed circuit, sketched in Fig. 8, has a 2-stage common source (CS) topology and inter-stage LC matching network. It has been designed in 65 nm CMOS SOI. Even though a cascode topology is normally more efficient for achieving high gains than CS topology, at low-voltage operation (1.2 V in our case) stacking the CS and the CG as in the cascode approach would determine a limited output voltage-swing thus compromising the OP1 dB (output power 1 dB compression point) of all the transmission system. The problem can be solved employing a folded-cascode topology and cascading several stages but the power consumption is nearly doubled vs. conventional cascode. Therefore, the proposed 2-stage CS topology has been selected as the most suitable in terms of trade-off between gain, linearity, power cost and output swing. The PA circuit in Fig. 8 exploits the benefit of the invariance of the maximum linearity bias current density (0.3 mA/μm) across technology nodes. The value of Jopt was found in Dickson et al. (2006) and remains constant for different finger widths and technology nodes (Voinigescu et al. 2007).

Fig. 8

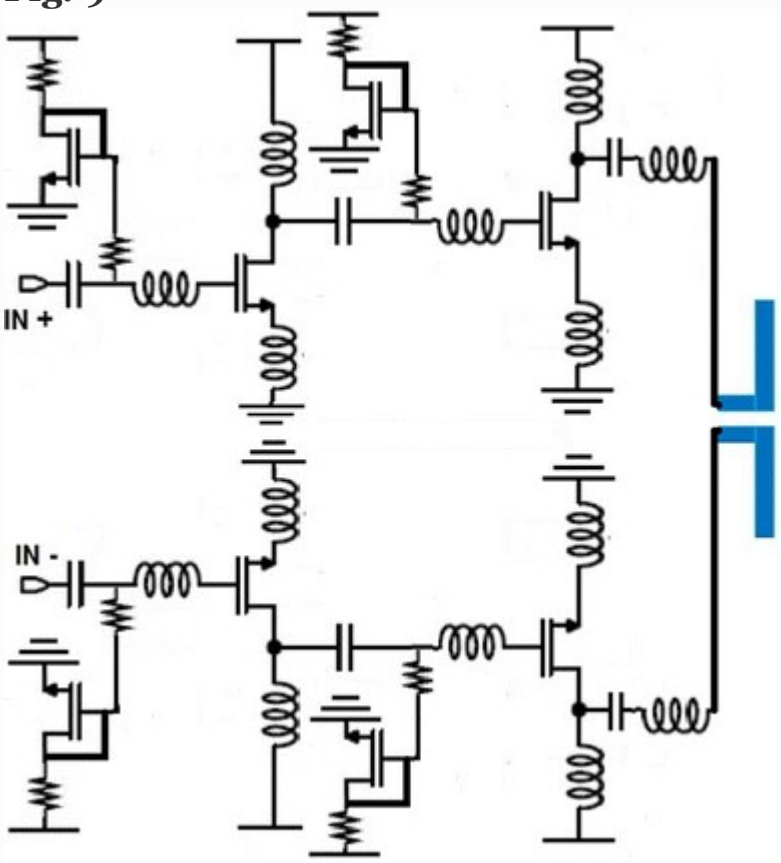


Single branch 2-stage CS power amplifier circuit

With a 1.2 V power supply the PA circuit in Fig. 8 has a gain of 7 dB at 60 GHz varying from roughly 8 dB at 57 GHz to 6 dB at 66 GHz. The 1-dB output and input compression points amount to 8.2 dBm (OP1 dB) and 1.76 dBm (IP1 dB) respectively. The DC power cost is 44 mW. The peak PAE (power-added-efficiency) is 11.5 %. The return loss (S_{11} parameter) is always below −10 dB, in the target 57–66 GHz spectrum. The stability factor is $K > 4$ for all the frequencies from 57 to 66 GHz, resulting in the unconditional stability of the two-ports network. The area occupation of the PA circuit (die area excluding pads) is about 0.11 mm^2.

To meet the 10 dBm system-level specification of Sect. 2.2 the transmit power of 2 PA blocks of Fig. 8 is combined in a pseudo-differential mode in the circuit of Fig. 9. This circuit topology is suited if the antenna has differential feed, as in case of the proposed dipole antenna designed in Sect. 4 with coplanar stripline feed. In case of single-ended antenna feed, the combination of power of 2 PA blocks can be alternatively realized through a Wilkinson Power combiner. As a result, the OP1 dB of the whole power amplifier in Fig. 9 in 65 nm CMOS SOI is 11.2 dBm. The resulting area occupation and the DC power cost are 0.22 mm^2 and 88 mW respectively.

Fig. 9



Pseudo differential power amplifier circuit

Table 3 compares the achieved results for the PA to recent works in literature (Siligaris et al. 2011; Abbasiet 2010; Wei et al. 2013; Raczkowski 2009; Juntunen et al. 2010; Lee et al. 2010) in terms of OP1 dB: i.e. in terms of the delivered output power in the linear region where distortions vs. an ideal linear amplifier are less than 1 dB. Our circuit solution of Fig. 9 allows for best performance in terms of OP1 dB, 11.2 dBm as in Abbasi et al. (2010), but using a lower supply voltage, 1.2 V instead of 2 V in Abbasi et al. (2010). Using in our case for the PA the same supply voltage of all the other blocks, including also the baseband and digital circuitry, reduces the overall system complexity avoiding extra DC–DC converter in the power management unit.

Table 3 1 dB compression point output power vs. state-of-art

Transceiver performance

Taking into account the whole transceiver architecture proposed in Sect. 2.2, and the key blocks designed and selected as most suited in Sect. 3 (2-stage LNA), Sect. 4 (dipole antenna) and Sect. 5 (2-branch PA), a complete mm-wave transceiver was implemented in 65 nm CMOS SOI technology with 1.2 V voltage supply. The achieved results are compared to recent state of art (Saponara et al. 2012, 2014; Juntunen et al. 2010; Lee et al. 2010; Byeon et al. 2013; Saponara and Neri 2015; Kang et al. 2009, 2010). As overall performance, the whole transceiver has an area occupation (die area) of about 2 mm^2, dominated by the area of the antenna, while the power cost is limited to 110 mW, dominated by the contribution of the PA. The proposed transceiver has been used to test a connection link between 2 nodes placed at different distances from few cm up to 10 m in a line-of-sight scenario. Indeed, as proved in Yilmaz et al. (2014) in case of a short-range (i.e. d < 10 m) 60 GHz link for home/office scenarios, line-of-sight propagation can be assumed. For one node the transceiver has been configured as transmitter, while for the other it has been configured as a receiver. The transmitter is connected to a digital source sending digital symbols in ASK configuration. The received symbols are stored at receiver side and then the two files of transmitted and received symbols are compared to determine erroneous bits and hence to derive BER (bit error rates) statistics. At the maximum distance of 10 m the following metrics have been derived: BER of 10^{-5}, energy per bit to noise ratio (E_b/N_o) of roughly 4 dB, bit-rate for each channel of 2.16 GHz of 800 Mb/s. A total data-rate of 3.2 Gbps can be achieved for the 4 channels available for the whole 57–66 GHz spectrum in Fig. 1. The channel-coding scheme used for this test was a Reed-Solomon convolutional one. The achieved results are well suited for data transfer in sensor or actuator networks and complex feedback systems such as CPS with real-time M2M or HMI interfacing. At lower connection distances, the BER performance improves (BER of 10^{-6} at roughly 3 m, 10^{-12} that is almost error-free at 1 m) and the proposed technology is also suitable for high definition multimedia data transfer.

Table 4 compares the performance of the proposed transceiver vs. recent ASK/OOK 60 GHz transceivers in state of art (Saponara et al. 2014; Saponara and Neri 2012; Juntunen et al. 2010; Saponara and Neri 2015; Kang et al. 2010), realized in silicon technologies, adopting on-chip antenna solutions. The comparison is done in terms of spectrum range, NF of the receiver, OP1 dB of the transmitter, link performance (data-rate and distance for which a BER lower than 10^{-5} is guaranteed), die area, power consumption. Table 5 compares the performance of the proposed transceiver vs. recent works (Lee et al. 2010; Byeon et al. 2013), adopting off-

chip antenna solutions in terms of antenna performance, OP1 dB of the transmitter, link performance (data-rate, distance), die area, power consumption. To be noted that all works refer to line-of-sight connections, which a valid assumption for 60 GHz links up to 10 m as proved in Yilmaz et al. (2014).

Table 4 Transceiver comparison vs. state-of-art with on-chip antenna

Table 5 Transceiver comparison vs. state-of-art with off-chip antenna

With respect to works such as Byeon et al. (2013), Kang et al. (2009, 2010) optimized for extremely low-power operations below 100 mW, our work has a slightly higher power cost (110 mW) but allows for a connection distance up to 10 m while the others are limited to much lower connections distances of 10 cm. Moreover, the solution proposed in this work is the only one covering the whole range of 9 GHz freely available worldwide (see Fig. 1). With respect to Saponara et al. (2014); Saponara and Neri (2015) having a similar transmitter configuration, this work minimizes the area occupation by adopting a time-division scheme where the same antenna is shared between the transmitter and the receiver.

The classic off-chip antenna solution can allow for higher antenna gains (e.g. 14 dBi for the off-chip patch array in Lee et al. (2010) while our on-chip dipole antenna has a gain limited to 3.05 dBi) but the performance achieved by the transceiver proposed in this work allows for the following advantages. The 50 Ω constraint is removed; the effect on the design of off-chip capacitive and inductive loads between the transceiver and the antenna is reduced; more compact sensor or actuator nodes can be realized since the antenna has not to be printed on the electronic board, occupying extra area, but is already included in the integrated RF circuitry.

Conclusions

The paper presented the design of key blocks (LNA, PA, antenna) for a mm-wave transceiver in 65 nm CMOS SOI technology and its comparisons to state of art. The proposed circuit solutions allow for the design of fully integrated transceiver enabling high speed networking in WSAN and CPS applications. The full integration approach minimizes the node size. With respect to state-of-art circuits at mm-waves, this work is the first proposing designs where the amplifiers are co-designed and co-optimized with the on-chip antenna. The sustained communication distance and data rate (3.2 Gbps at 10 m, BER lower than 10^{-5}) is suitable for WSAN and CPS

applications in home/office scenarios, or on-board vehicles (cars, trains, satellites, ships, airplanes) or body area sensor networks (for healthcare and wellness).

As far as adherence to the ECMA-387 (also ISO/IEC 13156) standard is concerned, the PA and the LNA blocks proposed in the paper, thanks to their performances can support all configurations foreseen in the physical layer of ECMA-387 and ISO/IEC 13156. Indeed, PA and LNA feature a wide bandwidth from 57 to 66 GHz, high linearity (e.g. the PA has an OP1 dB of 11.2 dBm), low return loss (the S11 parameter is below −10 dB for the whole spectrum range from 57 to 66 GHz), high gain and low NF for the LNA, higher than 15 dB and lower than 5 dB respectively. The LNA and the PA can be integrated as hard macro cells at layout level in a more complex system-on-chip communication terminal, fully compliant with ECMA-387 (ISO/IEC 13156). Considering the whole transceiver in Fig. 2, which integrates the LNA and PA in a scheme with single carrier transmission and non−coherent receiver, it will support a subset of the possible standard configurations (basic single−carrier transmission with modulation schemes like OOK or ASK).

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