Limits of sensing and storage electronic components for high-reliable and safety-critical automotive applications

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***Abstract*- The paper critically reviews the limits, for safety-critical automotive applications, of state-of-art technologies for non-volatile memory data/instruction storage and MEMS inertial sensors. Some hints, supported by theoretical analysis and/or experimental measures, to overcome these issues are provided. The reliability limits of plastic packages, typically adopted to keep low the device cost in the large volume automotive market, are also discussed. By exploiting a Fault Tree Analysis, the packaging bottlenecks are highlighted and proper countermeasures at circuit and technology level are proposed.**

***Keywords*- MEMS (micro-electro-mechanical-system), safety critical automotive applications, memories, package**

I. INTRODUCTION

Automotive driving assistance systems (ADAS) require high performance electronic components, able to operate in harsh environments and to guarantee fault robustness and functional safety. The large volume automotive market, 80-million vehicles sold worldwide each year, is well suited for the use of microelectronics and MEMS technologies. Key elements of ADAS are: i) the on-board motion sensors, such as accelerometers and gyroscopes to estimate the vehicle dynamics and stability, and to improve the accuracy of the position and navigation system (limited to some meters if relying only on GNSS satellite systems); ii) high-reliable microcontroller units with embedded non-volatile memory (NVM) to implement in real-time sensor fusion or control algorithms, whose computational burden is continuously increasing. Memory and sensor components are core products of semiconductor industry in Italy (e.g. ST, Micron, Invensense, Infineon, AMS). These devices have been originally developed for comfort or infotainment car applications, and their application to active safety and autonomous driving is not straightforward. To this aim this paper critically reviews motion sensors, memory components, the use of low-cost plastic packages, and highlights their performance and design bottlenecks. Hints to outcome such limits are also provided. Hereafter, Section II proposes new NVMs to achieve high-reliable instruction and data storage. Section III highlights the performance limits of on-board motion sensors. Section IV, through a Fault Tree Analysis (FTA), discusses the reliability of plastic packages, often used in automotive for their low-cost. Conclusions are drawn in Section V.

II. HIGH-RELIABLE NON-VOLATILE MEMORIES

Automotive applications require storage platforms for instructions and data with stringent reliability constraints The biggest issue is related to the high temperatures (up to 200°C) reached in some *under-the-hood* worst-case scenarios that severely threaten the non-volatility of the stored data. Typical NVM are designed in the front-end of the semiconductor process and can operate below 125°C guaranteeing the data storage for few years at that temperature only for a very low write cycling count (i.e., the measure of the memory lifetime wear-out due to repeated data writing and erasing). Embedded solutions based on the EEPROM concept have been developed in the mid '00s to cope with the temperature issue [1]. Multi-kbits memory modules functionality, and data retention of over 30 years for the automotive temperature range, have been achieved by a dedicated cell design in a 0.35 µm process [1, 2]. Moreover, write cycling of over 200k writes, tested up to 180°C, has been demonstrated, proving the suitability in all applications requiring frequent data manipulation and storage. The drawbacks of these solutions lie on the write and erase times (i.e., few milliseconds) and on the limited storage density.

In fact, the increased amount of sensors integrated in the car calls for denser NVM where calibration and real-time parameters must be safely stored, while at the same time providing fast response times for the system. To this extent, memory technologies integrated in the back-end of the semiconductor process could represent a viable solution. Magnetic Random Access Memories (MRAM) are one of the most promising candidates to replace traditional Flash in future NVM generations [3]. Among the MRAM paradigms under investigation in these years, the Thermally Assisted Switching (TAS) represents a good candidate for a replacement of standard embedded flash memories in automotive environments [4]. The mechanism of writing and erasing data into the memory cell of a TAS-MRAM is the following: small current flows through the Magnetic Tunnel Junction (MTJ) and heats the cell to the critical write temperature, concurrently to the application of a magnetic field aimed to polarize the storage layer of the cell. Then, the MTJ is cooled while write or erase field (i.e., the polarity of the field determines the operation type) is applied, essentially "freezing" the magnetic state into the storage layer. The magnetic orientation of the sense layer is irrelevant during write operation. By including a thermal barrier inside and around the MTJ to maximize the incremental temperature, it is possible to achieve data retention at high temperature and endurance capabilities to be exploited in harsh environment scenarios. Further, the write and read speed of these memories amounts to few hundreds of nanoseconds, making them appealing for many-sensors applications. To read the TAS memory state there are two known approaches: the Fixed Reference (FR) read and the Self Reference (SR) read, see Fig. 1. In the FR case, reading is achieved by measuring the absolute electrical resistance of the MTJ. This is possible by comparing the measured resistance with a reference resistor, hence its designation as "fixed reference". The performance figures of this technological option have been evaluated for automotive environments in state-of-art [5-7]. Despite the good reliability envisioned, there are still some issues in terms of data

retention properties at high temperatures that should be carefully evaluated. In the SR case, read is achieved by measuring the MTJ resistance twice. The first measurement is performed with the sense layer aligned in one direction and the second measurement in the opposite direction. The alternative alignment of the sense layer is achieved by first driving a "north" current in the corresponding filed line followed immediately by a "south" current, which can be achieved in a 5 to 10 ns time lapse. The magnitude of the field line current required to align the sense layer is similar to the field line current required for the write sequence. The power applied to the MTJ during read sequence is approximately one tenth of the power applied during write sequence. Consequently, there is no risk of unwanted write due to self-heating during read. The SR read therefore enables a very robust memory cell with extended reliability features that makes it attractive for automotive environment.

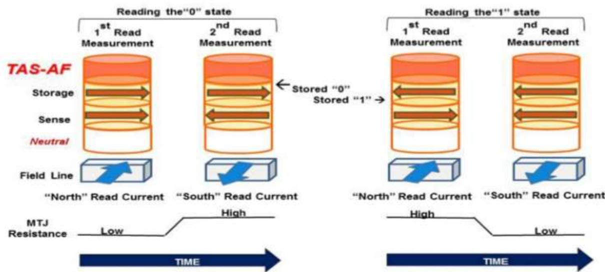

Fig 1. SR TAS-MRAM reading approach enabling very robust memory cells for automotive environments

To assess the capabilities of these memories we have tested a 1kbits SR TAS-MRAM memory array from Crocus Technology integrated in the back-end of a CMOS process. The cell and the test array architecture are made by: the MTJ device, composed of two ferro-magnetic layers separated by an insulating layer; three sense pads used during read operations to retrieve the memory content; two field-line drivers (FLDM, FLDP) to select the polarity of the field-line current in order to switch and read the memory. To change the state of a memory cell, two different writing operations are available: Write ’0’ (W0) and Write ’1’ (W1). Both operations require two voltages: VFORCE is required to heat the magnetic material, whereas VSWITCH allows changing the magnetic field polarization after heating. All write operations have been performed with TFORCE = 500ns and TSWITCH = 600ns. All read operations have been performed with VFORCE = 0.3V, TFORCE = 10μs and imposing a 40 mA field-line current. To evaluate the cells performance and reliability during cycling and the effect of the cell degradation, 500k Write ‘0’ and Write ‘1’ operations have been performed at room temperature. Fig. 2 shows the average and standard deviation values of the differential read resistances calculated after Write ‘0’ and Write ‘1’ operations during cycling on the full array. The data are plotted in terms of the differential resistance evolution, where this parameter is calculated as the difference between the read resistances measured when the field line voltage is applied on FLDP and FLDM, respectively. No sign of cycling wearout are visible after 500k operations. Concerning the data retention properties of the memory, the temperature-induced degradation has been evaluated by baking ceramic packaged test chips using both fresh and 500k cycled devices at 160°C for 150 h and then at 200°C for 100 h, see Fig. 3. No relevant impact of the retention tests is observed. A larger read window (i.e. the distance between the measured differential resistances after write operations) and lower standard deviation were observed on fresh devices. However, the retention tests do not cause any relevant variation of the memory content even when the samples are worn-out by a heavy cycle count.

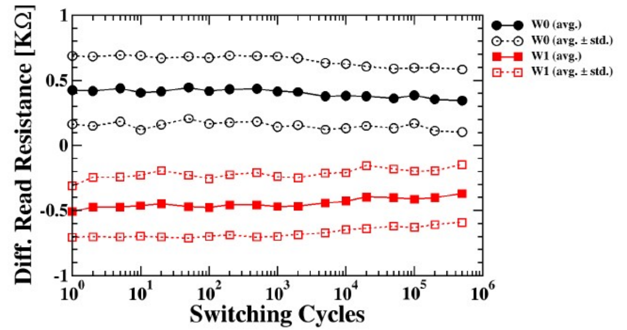

Fig 2. Average value and standard deviations of the differential read resistances measured after WO and W1 operations during 500k endurance cycles in SR TAS-MRAM arrays

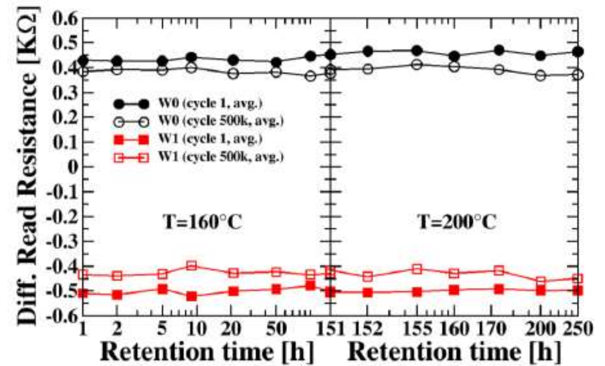

Fig 3. Average values of the differential read resistances measured after WO and W1 cycles during 150h of retention at 160°C and 100h at 200°C

III. Safety-critical application of inertial MEMS

MEMS inertial sensors (accelerometers and gyroscopes) are a well-established technology. First commercial accelerometers were available by Analog Devices since the mid ‘90s, and commercial gyroscopes by Bosch (angular rate sensors) lagging few years later [8]. The first automotive applications (crash detection for air bag control for accelerometers, electronic stability control for gyroscopes) were not highly demanding in terms of sensor performances, a fact that allowed development of very low cost devices in high volumes.

By mid ‘00s, the availability of low-cost, single-package, 3-axis accelerometers enabled many consumer applications, from videogame controllers to smartphone gesture recognition. Consumer applications became the driving force behind inertial MEMS market expansion in the following years, with many new players entering the field. Today, consumer-grade MEMS IMU (inertial measurement units) with 6 DOFs (3-axis acceleration and angle rate) or even 9 DOFs (adding 3-axis magnetic field measurement), such as ST LSM9DS1 or Invensense MPU-9250 are available at a retail price of a few dollars, and it is assumed that every smartphone contains one.

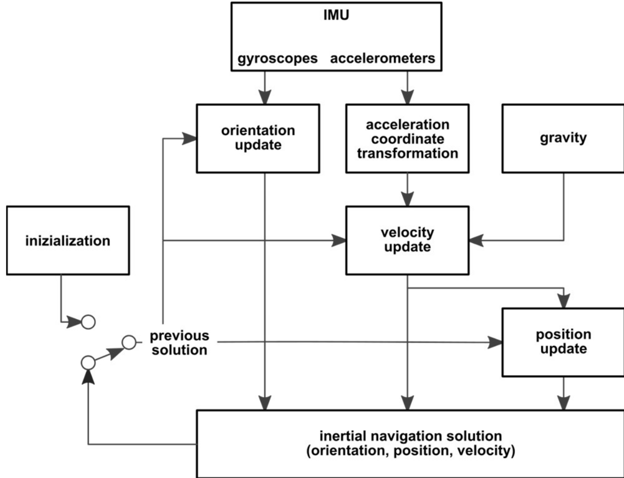

Fig 4. Block structure of an INS (adapted from [9]).

In contrast, the exploitation of inertial MEMS to some automotive applications, for which they were envisioned as an enabling technology since the MEMS beginnings, has proven elusive. Among these applications, accurate navigation, essential for autonomous driving, is the most prominent. As implemented in an Inertial Navigation System (INS), the accurate determination of position, velocity and orientation rely on the accuracy of the IMU around which the INS is built. Position and orientation are determined from the previous solution by integrating (once or twice) the acceleration and angle rate data from the IMU (Fig. 4). The INS solution can be integrated with the solution from a satellite-based system. Because of this double integration, the solution is extremely susceptible to many sources of error intrinsic to the MEMS sensors. Each sensor shows an offset (or *bias*), with a temperature-dependent component. Bias is given in *mg* for accelerometer, and *degrees/h* for gyroscopes. In presence of bias, the INS solution at rest drifts with time. IMUs are conventionally classified in different grades depending on their maximum bias (Table 1).

Highest grades cannot currently be reached with MEMS sensors, and are confined to high-value, low volume applications (aerospace, defence), where a single IMU can easily cost tens or even hundreds of thousands USD. Because of integration, the error on the estimated position caused by accelerometer and gyroscope bias increases quickly with time (as the second and third power of time, respectively), and grows to unacceptable levels for inertial navigation purposes. This is exemplified by Table 2, which gives a simplified error estimate after ten seconds for the different IMU grades. To move current MEMS inertial IMU to tactical on even higher grades, reliable in-run calibration techniques are mandatory [12]. Electronic calibration [13, 14] allows for compensating the effect of temperature on bias, as well as part of the effect of fabrication imperfections for a limited increase in complexity and cost. Mechanical calibration requires periodic controlled rotation along one or more axes, and while clever solutions allow mechanical calibration in specific applications [15], this approach is incompatible with low-cost systems. Continuous improvement of low-cost calibration techniques will probably play a role in future high-performance MEMS inertial systems [12]. Reduction of bias for low-cost MEMS also passes through better control of process variability, achieved through statistical process control methods [16].

TABLE 1. IMU GRADES BY BIAS VALUES, ADAPTED FROM [9-11]

IMU grade	Acceleration bias (mg)	Angular rate bias (deg/hr)
Strategic	$10^{-3} – 10^{-2}$	$10^{-4} – 10^{-3}$
Navigation	$10^{-2} – 1$	$10^{-3} – 0.1$
Tactical	1 – 30	0.1 – 30
Consumer	>30	>30

TABLE 2. TEN-SECOND POSITION ERRORS DUE TO SENSOR BIAS FOR DIFFERENT IMU GRADES

IMU grade	Due to acceleration bias (m)	Due to angular rate bias (m)
Strategic	$< 0.5\times10^{-3}$	$< 8\times10^{-6}$
Navigation	0.5×10^{-3}-0.5	8×10^{-6}-0.8×10^{-3}
Tactical	0.5-15	0.8×10^{-3} - 0.25
Consumer	> 15	> 0.25

Inertial sensors are also affected by output random noise, typically expressed in terms of its noise spectral density (measured in $\mu g/\sqrt{Hz}$ for accelerometers, $deg/s/\sqrt{Hz}$ for gyroscopes). The effect of noise is such that, even at zero input, the standard deviation of the estimated angles and positions grow as a function of time as $t^{1/2}$ and $t^{3/2}$, respectively. Intrinsic noise limits for inertial MEMS have always been the subject of intense research and, not surprisingly, higher noise levels are linked to higher thermo-mechanical losses in the MEMS component. However, electronic noise in the readout circuit gives an essential contribution to the final noise performances [17].

At least for MEMS gyroscopes, there is evidence that the currently adopted technology, based on the so-called tuning-fork Coriolis principle and capacitive (i.e. electrostatic) driving and sensing, is getting closer to what looks as a hard limit for noise, at around and above 10^{-3} $deg/s/\sqrt{Hz}$ [18]. Analysis of datasheets of commercial devices in Fig. 5 shows that the noise floor for consumer market gyroscopes has been close to this limit for several years now. The future roadmap to very low noise gyroscopes is currently not set, and several alternative approaches are researched. Without abandoning the mechanical structure of the tuning-fork Coriolis gyroscope, an improvement in noise floor has been demonstrated for piezoresistive, instead of electrostatic, detection [19].

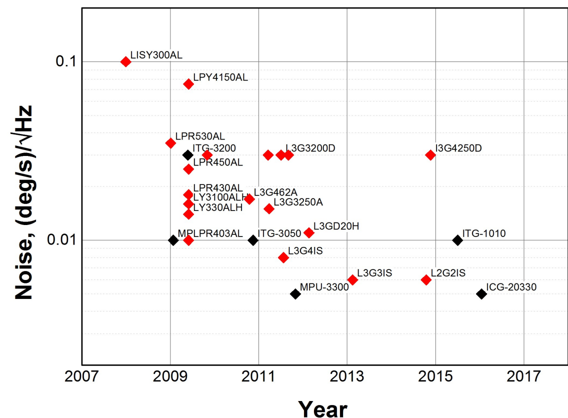

Fig. 5. Noise spectral density of several recent different commercial gyroscopes, by year. Color marks the supplier (red = STMicroelectronics, black = Invensense).

Piezoresistive sensing, however, comes with its own problems of linearity and temperature stability. Electrostatic (or piezoelectric) resonant bulk-mode gyroscopes, operating at relatively high frequency (around two decades above tuning-fork gyroscopes, which operate at tens of kHz), exhibit an intrinsically lower mechanical noise, which is however, only a part of the total output noise [20, 21]. There is also research on a different class of devices based on precession, the Rate-Integrating Gyroscopes (RIGs), whose output is directly proportional to the orientation angle, and not the angle rate [22]. This feature should reduce the impact of bias and noise significantly, as integration of the output can be avoided. RIGs, are still in their infancy, and their potential is still not clear.

III. HIGH-RELIABLE AND LOW-COST IC PACKAGING

The trend toward intelligent transportation systems and vehicles has forced the use of more complex system-on-chip, with increased number of memories and processing/sensing functionalities. Therefore, the number of I/O pins has been increased as well as the adoption of plastic package devices (PPD) [23-27] for their lower cost in the large automotive market vs. metallic or ceramic packaging. The market of most used packages (data extracted from the data-base of the main components distributors and from leader semiconductor companies [28-30]), is dominated (about 50%) by QFP (Quad Flat Pack) devices, including its Thin and Low-Profile variants, knowns as TQFP and LPQFP, respectively. Ball Grid Array (BGAs) solutions account for 30% of the market, including variants such as Fine-pitch (FBGA), Low-profile (LBGA), Low-profile Fine-pitch (LFBGA), Mold Array Process (MAPBGA). For devices that require a higher number of pins, BGA packages are preferred for their pin density, i.e. their more favourable ratio (number of pins)/area. Other types of package account for the remaining 20%. The higher the I/O Pin count, the higher the package size and complexity and hence the higher the reliability issue.

In automotive applications, to find the right trade-off between reliability of the PPDs and cost of technology/circuit solutions to achieve it, a FTA is proposed. In the FTA, a specific failure mode is considered as "top event". The FTA structure puts in evidence the failure logical relationship between faults and their causes. To provide quantitative useful hints for reliability countermeasures the FTA should take into account the failure distribution, i.e. the probability that a failure event happens. The higher the probability, the higher should be the action to reduce it. However, defining which are the top events of interests and the relevant FTs is not straightforward: only the most interesting and probable ones have to be modeled, or the FTA becomes too complex and un-useful since the main target in large volume vehicle electronics is keeping the device cost low. In this work, focusing on low-power ICs, and taking care of data reported in literature and laboratory experiments, two main FTs are proposed in Figs. 6 and 7. They consider separately two main failures "Open failure" and "Short failure". The "Open failure" in Fig. 6 takes into account the failures due to the interruption of the signal or power supplies. The "Short failure" in Fig. 7 takes into account the failures created by the connection of signal paths each other, or with the power supplies. This is the case of failures such as stuck at voltage supply (VCC) or ground (GND). Table 3 shows the distribution of faults for the FTA, which has been derived by mixing data from the analysis of real components in the market and experimental data after stress test in laboratories on QFP and BGA PPDs.

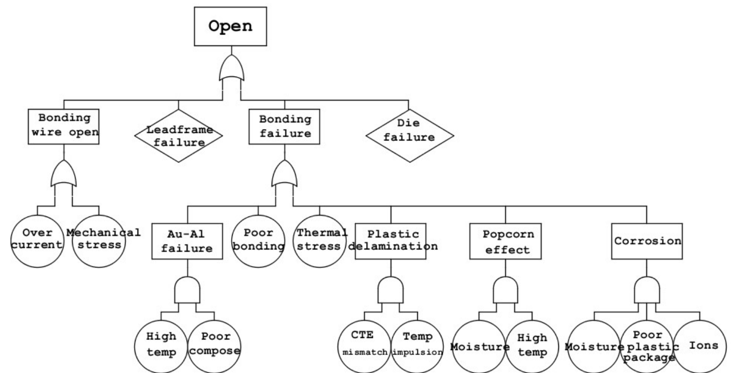

Fig. 6: Analysis of FT for "open" faults

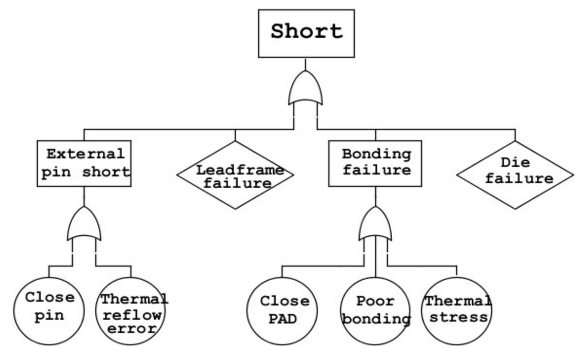

Fig. 7: Analysis of FT for "stuck at" faults

Considering the data in Table 3, this paper derives the probability of open or stuck at failure, under some assumptions verified by lab tests:

1) The die failure entries in Figs. 6 and 7 are calculated as the sum of the contribution of die cracking, die damage and wafer defects in Table 3. These contributions can be considered as fair partition between open and stuck at.
2) The broken wires/bonds and lifted wires value in Table 3 contributes partially to the Bonding wire open in Fig. 6 and partially to the Bonding failure in Figs. 6 and 7. From experimental tests, we derived a reasonable partition of 2/3 due to Bonding failure in Fig. 6 and 1/3 due to Bonding wire open in Fig. 7.
3) External pin short can be reasonably considered with a low fail probability of few %.
4) The leadframe failure in Figs. 6 and 7 can be considered with a fail probability of 3% to open failure and 1% to short failure.

TABLE 3: % DISTRIBUTION OF FAULTS

Failure Mechanism	%	Description
broken wires or bonds, lifted wires	32	Failures seen at the second stitch bonds on the lead frame or substrates
Die cracking	16	Die chipping, passivation cracking or metal traces cracking in the die
Delamination and popcorn effect	13	Interface delamination, such as mold/die interface
die/wafer damage/ defects	12	Die surface damage or scratch
Package or substrate cracking	10	Organic substrate crack and solder mask cracks
Other	17	Other failures. e.g. solderability, foreign materials

With the previous assumptions, the FTA in Fig. 8 is obtained. Fig. 8 is a new contribution in state-of-art since it highlights that the open failure rate is the dominating cause of faults in PPDs, about 38.4%, while the short (stuck at) failure rate is about 26.1%. The remaining 35.5% is due to the contribution of other types of failure which are more intermittent and which are more linked to a degradation of performance rather than a denial of service: e.g. leakage current increase, threshold voltage shift, unstable operation, increase in thermal resistance, bond wire resistance fluctuation.

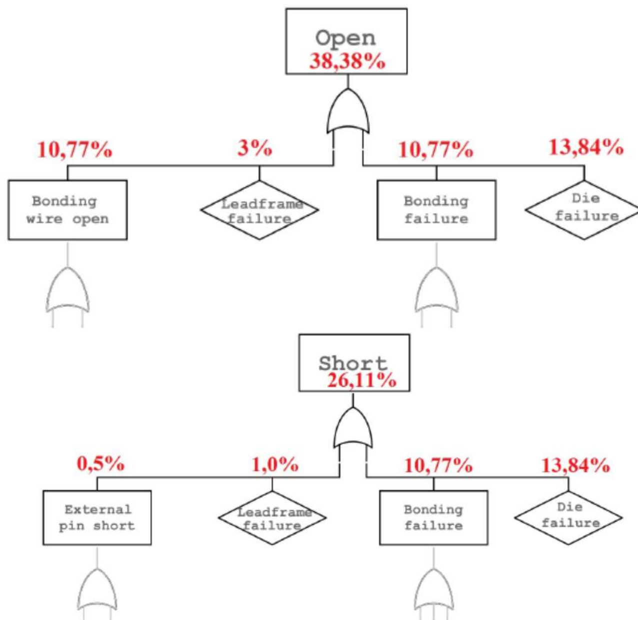

Fig. 8: Annotated FTA

Since from the above analysis bonding failure is the main cause of faults in open and stuck at FT_S, then we analyse countermeasures on it (die failure is not detailed since this section mainly refers to package issues). Bonding wire open, see Fig. 6, can be caused also by mechanical stress or overcurrent values. From our analysis, in low-power ICs such as microcontroller, sensor, memories this can happen mainly for the bonding related to power supply or ground pins.

To mitigate this issue two countermeasures can be adopted: first, at design time use all of free pins in the package for supply or ground; this way, given the same IC absorbed current, the current in each pin and the risk of overcurrent are reduced. Then, beside each voltage-clamping protection circuit, usually integrated on-chip in I/O interface blocks, a current monitoring system is used. Hence, when the current is above a given threshold the pin interface circuit is temporary switched off. Avoiding high current peaks, the pin and bonding are protected from damage, and when the current transient is again below the protection threshold, the pin functionality is restored. To avoid near-threshold intermittent phenomena a comparator with hysteresis is used: a low-cost solution, easy to integrate on-chip.

To avoid bonding failure from mechanical stress an accelerometer, tightly coupled with the IC to be protected can be used. When the acceleration becomes critical (i.e. over-threshold) the over-voltage and over-current protection circuits can be activated so that there is no power dissipation during the mechanical stress. This reduces the risk of damage since the thermal stress, and its synergistic effect with the mechanical stress, is removed. This countermeasure is cost effective only if the system already foresees the use on the same board, or in the system-on-chip, of an accelerometer.

Also technological countermeasures can be adopted. According to the statistical data in Table 3, percentage of wire-bonding resulting in IC's failure is about 32%. Typically, during the bonding Au-Al or Cu-Al a small portion of the Au wire is melt forming a ball as the wire material solidifies. The ball is pressed to the pad on the die with sufficient force to cause deformation and inter-diffusion of the wire and the underlying metallization, which ensures the contact between the two metal surfaces. The reliability of Au-Al bond in IC devices at high temperatures or currents is a key issue. The failure of Au/Al wire-bonding results in poor contact, wire shifting or failure off. The creation of Au/Al intermetallic compound and Kirkendall voids result in increasing of contact resistance and intermittently or permanent open failure mode. For the Au/Al bonding, there are five different intermetallic compounds that can form. These intermetallic elements are always present in Au/Al bonds but their concentration increases with high temperature and time. During the change of the temperature, the bond wires change their shape and the bond's mechanical strength increases. This may break the wire or divide the bond balls from the die pads so intermittently or permanently open appear. To improve the reliability of bonding, it is important the control of manufacturing equipment and the selection of materials to secure the initial joint properties. Unnecessary heating on semiconductor devices after the bonding process should be avoided, because Au goes into Al much faster than Al goes into Au. The result is an increase of vacancies at the Au side of the intermetallic stack. In the end of the useful life, bond's contact resistance increases, degrading the chip performance, and finally becomes open. The formation of Kirkendall voids principally depend on time, temperature and chemical concentration of the diffusion species. As a technological countermeasure, the problem with the intermetallic compounds (IMC) can be reduce using Cu wires instead Au wires. The IMC layers are fundamental for the bonding but these should be thin. IMC are fragile, with poor conductivity and lead to crack at the interface. Thicker IMC layers reduce the IC reliability and performance. As proved in Fig. 9, the AuAl IMC layer is thicker than CuAl.

Another common failure mechanism in PPDs is the Popcorn effect. It occurs when the device is rapidly exposed to high-temperature, as in reflow soldering, or when operating in harsh environments. At these temperatures the moisture absorbed by plastic materials in package suddenly vaporizes and expands resulting in rapidly increasing vapor pressure inside of package. When the high vapor pressure increases the void or defects along the interface will grow to result in delamination, and formation of cracks. When the crack reaches the package exterior, high-pressure vapor is rapidly released, producing an audible sound like popcorning. This effect can be close to die, going to move the die from the lead-frame, damaging the bonding wires. If the crack reaches the exterior other corrosive elements may get inside damaging the die and the bonding structures. Popcorning may result in immediate or long-term failure of the device.

The countermeasures to reduce the popcorn effect are:

- When components are stored is is important to control the humidity and temperature values.
- The devices must be used as soon as the moisture-proof pack (which should have a desiccant inside) is opened.
- Devices should be mounted on the board at a temperature as low as possible and in short time, while controlling the moisture absorption.
- The timing of the storage is an important parameter. If the devices are stored over the specific period need to be baked at 125 °C for 24 h (under nitrogen atmosphere). This reduces drastically the moisture absorbed and so reduces the risk of popcorning during the solder reflow.

When PPDs are applied to rapid temperature changed environment the mismatched coefficient of thermal expansion (CTE) between the molding compound and the lead-frame or die may cause delamination or crack between the surfaces. Especially the thermal expansion coefficient of molding compound (about $25 \cdot 10^{-6}$ °C^{-1}) is almost one order of magnitude larger than the silicon one. When the temperature changes, during the thermal solder reflow or other situation, the size change of package and chip will be greater which bring out stress. This stress may cause a weak adhesion on the chip pad bonding, and the shift of the bonding ball may create short circuit or open circuit. The shear stress may create crack under the die, between the plastic package and the die, leads to pockets of air that reduce the heat dissipation. The passivation peeled off and even damages the chip, resulting in device failure. As a countermeasure, to avoid the problems of CTE mismatch, materials with comparable CTE must be used.

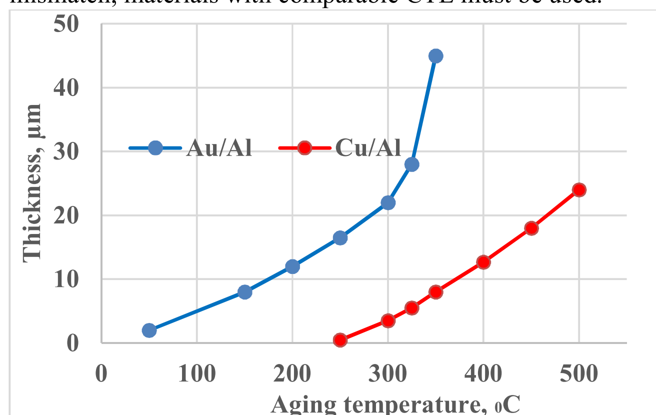

Fig. 9: Intermetallic growth. AuAl IMC layer thicker than CuAl

IV. Conclusions

The paper has critically discussed the main limits, for safety-critical automotive applications, of state-of-art technologies for NVM data/instruction storage and for MEMS inertial sensors. TAS-MRAM memory, integrated in the background of a conventional CMOS technology, has been proved as a valid alternative to conventional flash memories when fast (tens of ns access time) and reliable data/instruction storage has to be achieved at high temperature. Experimental measurements up to 200 °C are reported. As far as inertial MEMS is concerned, the paper shows that bias and output random noise of state-of-art accelerometers and gyroscopes, pose several limits on their application in high-reliable autonomous driving navigation, positioning and stability control. Technology solutions and calibration methods, to overcome these issues, are discussed. Finally, the reliability limits of plastic packages, adopted to keep low the device cost in the large volume automotive market, is analyzed. By exploiting a Fault Tree Analysis, the packaging bottlenecks are highlighted and specific countermeasures are proposed at circuit and technology levels.

References

[1] M. Thomas et al., "A non-volatile embedded memory for high temperature automotive and high-retention applications," IEEE ISQED 2006
[2] A. Chimenton et al., "Evidence of erratic behaviors in p-channel floating gate memories and a cell architectural solution," IEEE NVMTS 2009, pp.63-66
[3] W. Gallagher et al., “Recent advances in MRAM technology,” IEEE VLSI TSA Int. Symp. 2005, pp. 72–73
[4] I. Prejbeanu et al., “Thermally assisted MRAM,” J. Phys. Condens. Matter, vol. 19, 2007
[5] E. Wachmann et al., “ATHENIS-3D: Automotive tested high-voltage and embedded non-volatile integrated SoC platform with 3D technology”, IEEE DATE 2016, pp. 894-899.
[6] A. Grossi et al., “Reliability and cell-to-cell variability of TAS-MRAM arrays under cycling conditions”, IEEE NVMTS 2015
[7] A. Grossi et al., "Automated characterization of TAS-MRAM test arrays," 10th Int. Con. on Des. & Tec. of Int. Syst. in Nan. Era, 2015
[8] V. Kempe, *Inertial MEMS*. Cambridge: Cambridge University Press, 2011.
[9] P. Groves, *Principles of GNSS, Inertial, and Multisensor Integrated Navigation Systems*, Artech House, 2008.
[10]KVH white paper, “Guide to comparing gyro and IMU technologies”, 2014
[11]http://www.yole.fr/iso_upload/Samples/Yole_High_End_Gyro_January_2015_Sample.pdf, “High-end gyroscopes, accelerometers and IMUs for defence, aerospace & industrial,” Yole, pp. 1-25, 2015
[12] M. Perlmutter, S. Breit, “The future of the MEMS inertial sensor performance, design and manufacturing,” DGON Inertial Sensors and Systems (ISS), 2016, pp. 1–12.
[13] I. P. Prikhodko, et al., “Compensation of drifts in high-Q MEMS gyroscopes using temperature self-sensing,” Sensors Actuators A Phys., vol. 201, pp. 517–524, 2013.
[14] I. P. Prikhodko, et al., “In-run bias self-calibration for low-cost MEMS vibratory gyroscopes,” IEEE PLANS 2014, pp. 515–518
[15] J. Collin, “MEMS IMU carouseling for ground vehicles,” IEEE Trans. Veh. Technol., vol. 64, n. 6, pp. 2242–2251, 2015
[16] M. Schwarz, et al., “The future is MEMS design considerations of microelectromechanical systems at Bosch,” Proc. 22nd Int. Conf. Mix. Des. Integr. Circuits Syst. Mix. 2015, pp. 177–180
[17] F. Mohd-Yasin et al., “Noise in MEMS,” Meas. Sci. Tech., vol.21, 2010
[18] D. Serrano, “Integrated inertial measurement units using silicon bulk-acoustic wave gyroscopes,” PhD thesis, Georgia Institute of Technology, 2014.
[19] S. Dellea, F. Giacci, A. F. Longoni, G. Langfelder, “In-Plane and Out-of-Plane MEMS Gyroscopes Based on Piezoresistive NEMS Detection,” J. Microelectromechanical Syst., vol. 24, n. 6, pp. 1817–1826, Dec. 2015.
[20] R. Tabrizian, et al., “High-Frequency AlN-on-Silicon Resonant Square Gyroscopes,” J. Microelectromech. Syst., vol. 22, n. 5, pp. 1007–1009, 2013.
[21] M. Hodjat-Shamami, et al., “A dynamically mode-matched piezo electrically transduced high-frequency flexural disk gyroscope,” 28th IEEE Int. Con. on Micro Electro Mech. Sys. 2015, pp. 789–792.
[22] J. Cho et al., “High-Q, 3kHz single-crystal-silicon cylindrical rate-integrating gyro (CING),” IEEE Int. Con. on Micro Elec. Mech. Sys. 2012
[23] Huiwei Wu et al., "Failure analysis and case study of plastic encapsulated microelectronics," IEEE ICRMS 2014, pp. 70-73
[24] P. Lall et al., "Model for BGA and CSP Reliability in Automotive Underhood Applications", IEEE Tran. on Comp. and Pack. Teach., vol. 27, n. 3, 2004, pp. 585-593
[25] P. Dientrich et al. “Joining and package technology for 175°C Tj increasing reliability in automotive applications”, Microelectronics Reliability, vol. 54, n. 9-10, pp. 1901-1905, 2014
[26] Yue Liu et al., “Package reliability of MEMS sensors used in automotive under random vibration”, Chemical Eng. Trans., vol. 33, 2013
[27] M. Sendor, “Plastic encapsulated microcircuits (PEMs) reliability/usage guidelines for space applications”, D-19426 Jet Propulsion Lab, 2000, pp. 1-25
[28] Renesas, “Semiconductor Reliability Handbook”, 2013
[29] STMicroelectronics, “Soldering recommendations and package information for Lead-free ECOPACK microcontrollers”, 2016
[30] “Failure mechanism of semiconductor devices”, Panasonic, http://www.semicon.panasonic.co.jp/en/aboutus/pdf/t04007be-3.pdf