An Ultra-Low Voltage Energy Efficient Level Shifter

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***Abstract*—This paper presents an energy-efficient level shifter able to convert extremely low levels input voltages to the nominal voltage domain. To obtain low static power consumption, the proposed architecture is based on the single stage Differential Cascode Voltage Switch scheme. Moreover, it exploits self-adapting pull-up networks to increase switching speed and to reduce dynamic energy consumption, while a split input inverting buffer is used as output stage to further improve energy efficiency. When implemented in a commercial 180 nm CMOS process, the proposed design can up-convert from the deep subthreshold regime (sub-100mV) to the nominal supply voltage (1.8V). For the target voltage level conversion from 0.4V to 1.8V, our level shifter exhibits an average propagation delay of 31.7 ns, an average static power of less than 60 pW and an energy per transition of 93 fJ, as experimentally measured across the test chips.**

Index Terms—**differential cascode voltage switch, level shifter, subthreshold circuit.**

I. Introduction

Multiple supply voltage (MSV) [1] technique is gaining broad popularity for the design of advanced system on chips (SoCs). The MSV approach consists of partitioning (also dynamically) the design into separate voltage domains (or "voltage islands"), each operating at a proper power supply voltage depending on its timing requirements [1]. Time-critical domains run at higher supply voltage (V_{DDH}) to maximize the speed, whereas noncritical sections operate at lower supply voltage (V_{DDL}) to optimize energy. In this way, elaboration tasks that require substantially different performance capabilities are effectively managed [1]. Aggressive voltage scaling into the sub/near-threshold region for sections operating at V_{DDL} would provide a better use of the available energy budget [2]. One of the main challenges in the design of effective MSV SoCs is the minimization of delay and energy for level conversion between different voltage domains [3]. This issue becomes particularly critical when the number of power domains and/or the bus data width in the SoC increase.

Several level shifter (LS) circuits were recently proposed [4-18] to allow voltage conversion from the deep subthreshold regime up to the nominal supply voltage level. The LS proposed in [5] is based on the Wilson current mirror configuration. This circuit results to be fast at the expense of large standby power consumption [11], which is problematic for long period or low duty cycle applications. To manage static power issues, some modified Wilson current mirror-based LS circuits were recently presented in [11, 14]. However, static power consumption remains considerable. Differently from current mirror configurations, LSs based on Differential Cascode Voltage Switch (DCVS) structure have close-to-zero standby power consumption, due to the presence of complementary pull-up networks (PUNs) and pull-down networks (PDNs). Unfortunately, they suffer from the current contention occurring between the PUN and PDN during the output switching, which affects both the transition time and the dynamic power. The above effects are exacerbated when a low voltage input signal has to be up-converted to a significantly higher voltage level [6, 8, 12]. One obvious way to deal with this problem is to increase the strength of the PDNs relative to PUNs. However, some works [5, 6] demonstrated that the PDN transistors need to be upsized by several orders of magnitude in order to correctly overcome the strength of PUNs for converting from sub- to above-threshold voltage levels, which is often impractical. To solve the above issue, a two stage Differential Cascode Voltage Switch (DCVS)-based LS circuit was proposed in [6]. Although, the double stage topology facilitates wide-range voltage up-conversion, the conversion delay is increased with respect to a single stage DCVS-based structure. The single stage DCVS-based LSs presented in [8] and in [12] use diode-connected transistors to limit current contention at the critical discharging internal nodes during the output switching. A similar achievement is obtained in the LS circuit proposed in [10], through the use of two current generators. The design, previously proposed by one of the authors of this work [13], exploits a different idea based on self adapting PUNs to speed-up both high-to-low and low-to-high transitions of critical internal nodes.

In this work, we present the design of an ultra-low voltage energy-efficient LS in 180 nm CMOS and we validate it through measurements on fabricated samples. The proposed circuit exploits improved self adapting PUNs to achieve fast

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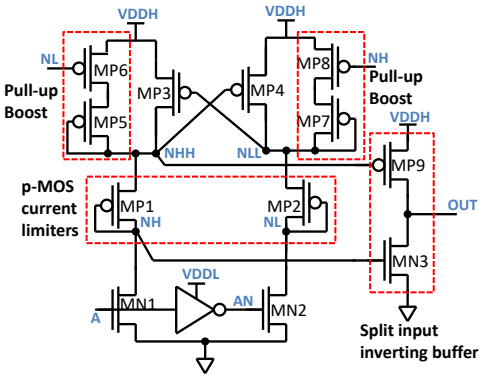

Fig.1. The proposed level shifter.

and energy-efficient conversion from deep subthreshold to nominal supply voltage domain, while a split input inverting buffer is used as output stage to reduce short circuit and stand-by energy consumption. Measurement results show that our design can up-convert from 50 mV to the nominal voltage of 1.8V. For a 0.4V input pulse, an average propagation delay of about 32 ns was measured across the test chips with stand-by power consumption smaller than 60 pW.

The rest of the paper is organized as follows: Section II describes the proposed LS design and provides a simulation-based comparative analysis. Section III presents the measurement results compared with previously published competitors. Finally, conclusions are given in Section IV.

II. Proposed Level Shifter and Simulation-based Comparison

A. *Proposed design*

As shown in Fig.1, the proposed design consists of an input inverter to provide differential low-voltage signals, a modified DCVS-based conversion stage, which is responsible of the voltage shifting operation and an inverting buffer designed to assure adequate output driving strength. The key improvements with respect to the conventional DCVS-based structure are highlighted in Fig.1. Two p-MOS diodes [4] (i.e. *MP1* and *MP2*), acting as current limiters, are used to mitigate the current contention at the beginning of *NH* or *NL* discharging transition. The output buffer is driven in a split way [9] by *NH* and *NHH* nodes, whose voltage values differ from the voltage drop (V_D) on *MP1*. This ensures that one of the devices (either the pull-up or the pull-down transistor) in the output inverter is completely turned OFF when the other turns ON. In this way, the short circuit current in the output buffer is significantly reduced with respect to the option used in [4, 8, 12-13], while the output switching speed is also improved. To further improve the charge and the discharge operations of the critical internal node, self-adapting PUNs able to dynamically adjust their strengths depending on the occurring output transition, were considered for the two branches of the conversion stage. For this purpose two pull-up boost circuits were introduced in parallel to the pull-up devices (i.e. *MP3* and *MP4*) of the conventional DCVS structure.

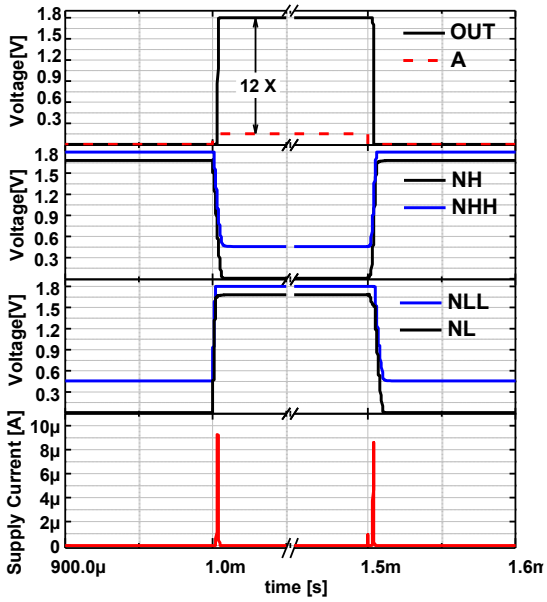

Fig.2. Simulated transient behavior of the proposed level shifter.

Fig. 2 better illustrates the behavior of the proposed LS with reference to the voltage up-conversion of an input voltage pulse amplitude from 150 mV to 1.8V. When the input signal *A* is low, the voltage on node *NH* is high (V_{DDH}-$V_{D,MP1}$) and the voltage on node *NL* is low (0V). A low-to-high (high-to-low) input signal *A* (*AN*) transition causes *MN1* (*MN2*) to be switched ON (OFF) and, consequently the *NH* node starts to be discharged. This operation is in a first phase greatly favored by the current-limiting action of *MP1* and by the presence of *MP2* which forms a voltage divider to keep the node *NLL* at a voltage higher than *GND*. In this way, $|V_{GS}|$ of *MP3 is* reduced and the pull-up of the left branch is weakened to allow faster discharging of node *NH*. As *NH* discharges through *MN1*, the pull-up boost of right branch turns ON (i.e. the pull-up of the right branch is strengthened), thus leading the *NLL* node to be fast charged towards the V_{DDH}-$V_{D,MP7}$ voltage. As a consequence, a positive feedback is triggered causing *MP3* to be completely turned OFF and *NH* to be fully discharged. At the same time the pull-up boost of the right branch turns OFF (i.e. the *MP7* diode becomes OFF) and *NLL* is raised to V_{DDH} through *MP4*. In this way, the voltage levels of the internal nodes are established to assure fast switching and reduced energy consumption in the subsequent input transition (i.e. the pull-up of the right branch is now weakened due to the reduced $|V_{GS}|$ of *MP4*). The proposed LS was designed for the 180 nm UMC CMOS technology and sized as reported in Table I.

TABLE I
Transistor Sizes

Transistor	W/L[µm]	Transistor	W/L[µm]
MN1	0.24/0.18	MP4	0.24/0.2
MN2	0.24/0.18	MP5	0.24/0.18
MN3	0.24/0.18	MP6	0.24/0.18
MP1	0.24/0.18	MP7	0.24/0.18
MP2	0.24/0.18	MP8	0.24/0.18
MP3	0.24/0.2	MP9	0.36/0.18

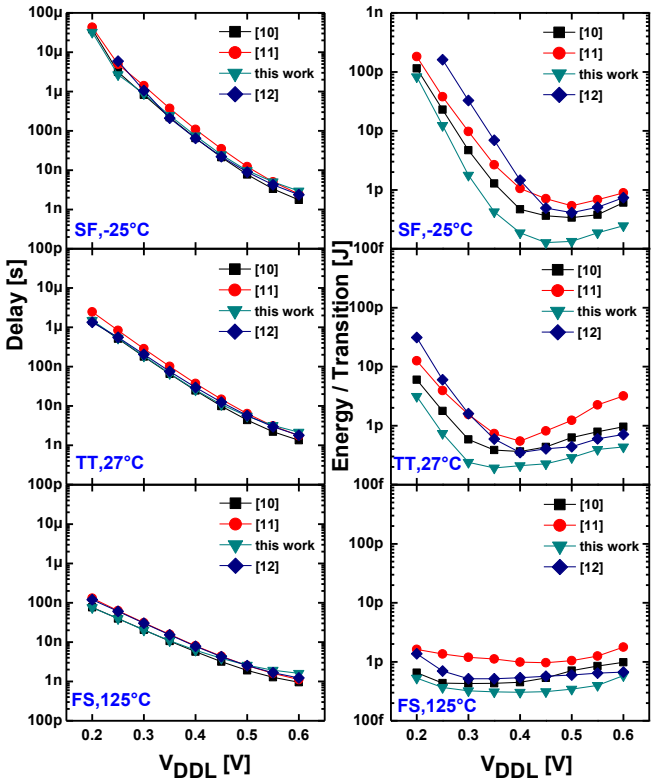

Fig.3. Delay-Energy characteristics versus V_{DDL} (@V_{DDH}=1.8V, Freq.100 kHz) evaluated for different process-temperature corners.

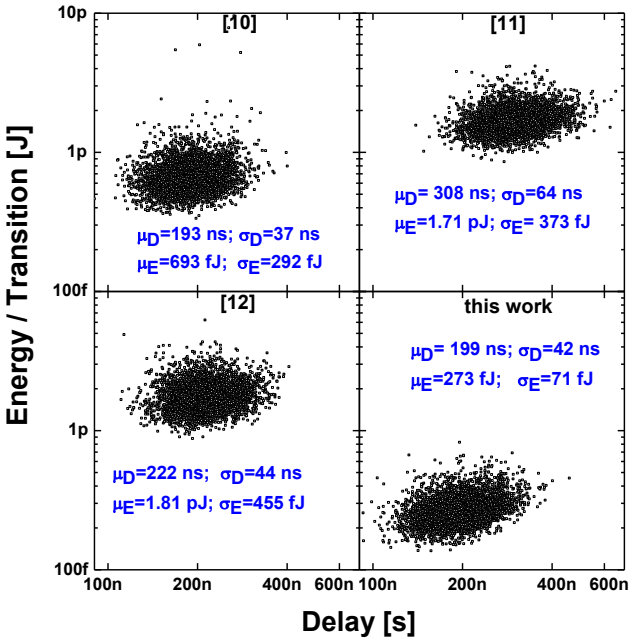

Fig.4. Monte Carlo comparison on 4000 runs (V_{DDL}=0.3V, V_{DDH}=1.8V, Freq.100 kHz, T=27°C)

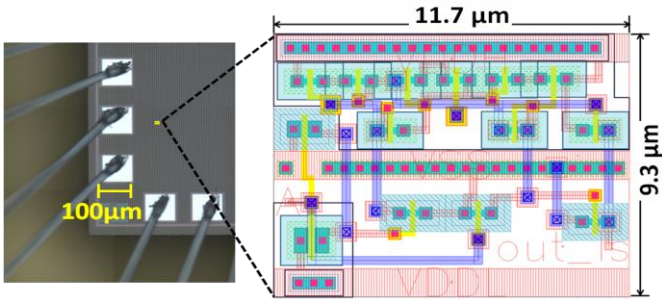

Fig.5. Micrograph of the testing chip and layout of the proposed level shifter.

Although the multi-threshold CMOS technique [12-13] can be exploited to emphasize the operating characteristics of the proposed LS, in our design, we used only regular threshold (RVT) devices to better evaluate advantages offered by the circuit topology without any interference from the V_{th} of the devices.

B. *Comparative Simulation-based Analysis*

In order to demonstrate the benefits of the proposed design, we performed a comparative analysis with three among the most efficient and recent LS proposals [10-12]. For the sake of fair comparison, we replicated the above designs in the considered CMOS process, while imposing a transistor length of 180 nm and maintaining the same W/L ratios indicated in the referenced papers. Also, all the compared circuits use only RVT devices.

Fig. 3 compares delay and energy per transition results for input voltage levels ranging from 0.2V to 0.6V. Simulations were performed for three different Process-Temperature (PT) corners and considering an input signal frequency of 100 kHz, V_{DDH} fixed to 1.8 V and an output capacitive load of 16 fF (corresponding to the input capacitance of 20 minimum-sized inverters in the adopted CMOS process). The typical PT corner involves both typical n/p-MOS transistors and a temperature of 27°C. The second corner was determined considering the worst case operating condition occurring when input signal is in the sub-threshold regime. In such a condition, the weakly driven n-MOS transistors (i.e. *MN1* and *MN2*) have to overcome the opposing p-MOS devices (i.e. *MP3* and *MP4*) to enable switching operation. Thus, slow n-MOS and fast p-MOS devices are used, while a temperature of -25°C was considered because it implies a weaker operation for *MN1* and *MN2* in the sub-threshold region. As opposite PT corner, fast n-MOS, slow p-MOS and a temperature of 125°C were taken into account. The circuit in [12], sized as before described, fails to operate properly for V_{DDL}=0.2V in the slow n-MOS and fast p-MOS process corner. In all the considered PT corners, both our design and the LS topology proposed in [10] lead to the smaller propagation delay in the sub/near-threshold regions (Vth≈0.32V for TT process corner at V_{DS}= 1.8V and T=27°C), while the proposed solution has proved to be always the most efficient in terms of energy consumption. To investigate the robustness of the proposed LS against device mismatch, we have performed a 4000-points Monte Carlo (MC) simulation. The related results are shown in Fig. 4. The normalized standard deviations (σ/μ) of the delay and of the energy consumption are 0.21 and 0.26, respectively. Such values are comparable to those obtained for the previous proposed circuits [10-12]. However, as can be easily observed in Fig.4, our design still remains the preferable choice due to

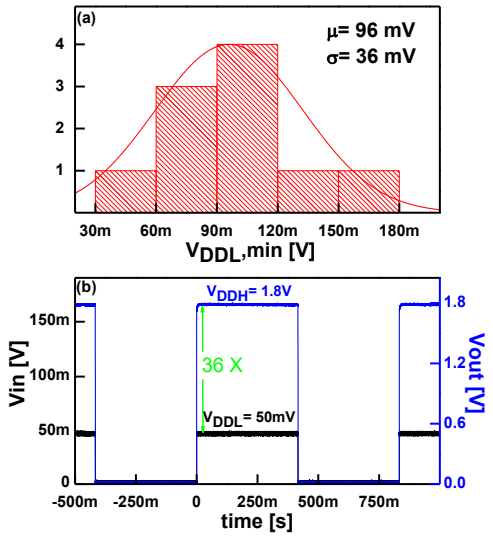

Fig.6. V_{DDL},min measurements: a) Distribution of minimum V_{DDL} for successful up-conversion to 1.8V; b) Measured waveform for a 50mV to 1.8V conversion.

the significantly reduced mean energy and competitive mean delay, coming from the use of self-adapting PUNs.

III. Measurement Results and Discussion

Fig. 5 shows the layout view of the proposed LS, which has been designed exploiting only metal-1&2 wires and following the double-cell-height strategy suggested in [18]. Power supplies are available through the top and the bottom metal-1 rails, while a shared metal-1 ground rail crosses the cell in the center.

We fabricated a proof-of-concept chip using the 0.18 µm, 1-poly, 6-metal UMC CMOS process. In such technology, the physical design of the proposed LS occupies a silicon area of only 108.8 µm^2 (11.7 µm * 9.3 µm). Static measurements have been performed on a set of ten samples at wafer level exploiting a probe station Cascade SUMMIT 11861B with AttoGuard technology. In particular, the static current was measured by means of the parameter analyzer Keithley 4200-SCS equipped with source measure units with preamplifiers, which extend the current range to 0.1fA resolution. On the other hand, a custom printed circuit board was fabricated for measuring the dynamic response of our LS. Delay measurements were performed on four packaged samples by stimulating the device under test through a RF waveform generator and using an active broadband probe connected to a 10 GSa/s Rohde&Schwarz RTO1044 digital oscilloscope. High bandwidth (DC–18 GHz) SMA-type cables were used for these experiments.

Fig. 6a shows the distribution of the measured minimum V_{DDL} for successful up-conversion to 1.8 V. The minimum up-convertible voltage level can be as low as 50 mV, while the worst case is 170 mV among the 10 characterized chips. Fig. 6b shows the measured up conversion to 1.8V for the best case 50 mV input pulse waveform.

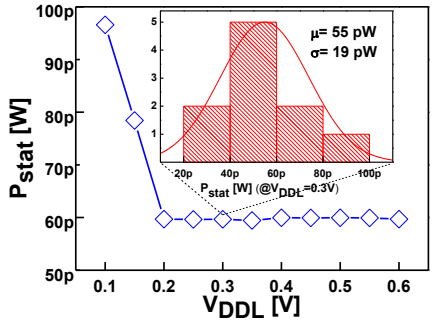

Fig.7. Measured static power versus V_{DDL}.

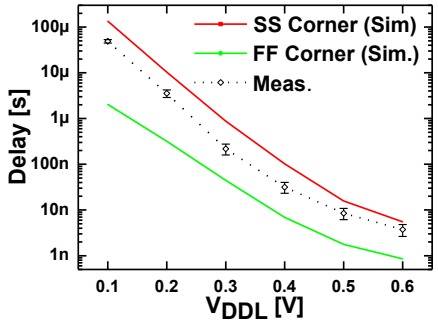

Fig.8. Measured delay versus V_{DDL}.

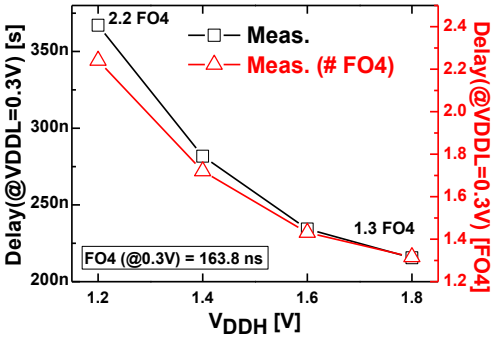

Fig.9. Measured delay versus V_{DDH}.

Fig. 7 illustrates the typical static power results evaluated for V_{DDH}=1.8V and V_{DDL} ranging from 0.1 V to 0.6 V. For V_{DDL} larger than 0.2 V the standby power consumption saturates to about 60 pW, thus demonstrating the suitability of the proposed LS also for long period or low duty cycle applications. By observing the insert of Fig. 7, it can be noted that the very low standby power consumption has been achieved with a normalized variation (σ/µ) lower than 20%.

Fig. 8 illustrates measurement results of the mean propagation delay for different V_{DDL}. In this plot, error bars are also reported as a measure of the uncertainty in delay measurement. The worst case delay is 49 µs when the input supply is 100 mV, whereas at V_{DDL}=0.6V the LS delay decreases down to 3.5 ns. The results given in Fig. 8 also show that the delay of our circuit is within the range predicted by the process variability evaluated using simulations.

TABLE II
COMPARISON WITH STATE-OF-THE-ART ULTRA LOW VOLTAGE LEVEL SHIFTERS

Design	Tech.	Conversion range	Delay (ns)	E_{tr} (fJ)	P_S (pW)	Area (μm^2)	Results
[7]	0.35 µm	0.23V - 3V	10^4 (0.4V→3V)	$5.8*10^3$ (0.4V→3V-10kHz)	230 (0.4V)	1880	Meas.
[4]	0.18 µm	0.13V - 1.8V	45 (0.4V→1.8V)	≈$2*10^3$ (0.4V→1.8V - 100kHz)	N.A.	N.A.	Meas.
[14]	0.18 μm	0.21V - 1.8V	≈167 (0.3V→1.8V)	39 (0.3V→1.8V-100 kHz)	160 (0.3V)	153.01	Meas.
this work	**0.18 µm**	**0.1V - 1.8V**	**31.7 (0.4V→1.8V)**	**93# (0.4V→1.8V-100 kHz)**	**55 (0.4V)**	**108.8**	**Meas.**
[6]	0.13 µm	0.18V - 1.2V	≈25 (0.4V→1.2V)	N.A.	N.A.	≈96	Meas.
[9]	0.13 µm	0.25V - 2.5V	58.8 (0.3V→2.5V)	191 (0.3V→2.5V- N.A.)	724 (0.3V)	71.94	Meas.
[11]	65 nm	0.165V - 1.2V	<162## (0.3V→1.2V)	136## (0.3V→1.2V- 20kHz)	N.A.	16.8	Meas.
[12]	65 nm	0.14V - 1.2V	25 (0.3V→1.2V)	30.7 (0.3V→1.2V- 1MHz)	2500 (0.3V)	17.6	Meas.
[11]^	0.18 μm	0.1V - 1.8V	37.2 (0.4V→1.8V)	598 (0.4V→1.8V-100kHz)	866 (0.4V)	N.A.	Sim.
[12]^	0.18 μm	0.2V - 1.8V	29 (0.4V→1.8V)	296 (0.4V→1.8V-100kHz)	1920 (0.4V)	N.A.	Sim.
[10]	0.18 μm	0.1V - 1.8V	≈30 (0.4V→1.8V)	≈250 (0.4V→1.8V-1MHZ)	130 (0.4V)	120.9	Sim.
[15]	0.18 μm	0.19V-1.8V	21.6 (0.4V→1.8V)	390 (0.4V→1.8V-100kHz)	160 (0.4V)	95.6	Sim.
[16]	0.18 μm	0.32V-1.8V	31 (0.4V→1.8V)	680 (0.4V→1.8V-1MHZ)	1160 (0.4V)	N.A.	Sim.

#simulated data ## data reported in [14] ^ replicated in this work

Fig. 9 shows the measured average delay for different V_{DDH} and for V_{DDL}= 0.3V. In addition to the measured absolute delay values, the FO4 delay is also plotted (the unit-FO4 delay was obtained by simulations for V_{DD}=0.3V and T=27 °C). As V_{DDH} increases, the delay decreases mainly due to the decrease of the output inverting buffer delay.

Table II compares the proposed circuit with several state-of-the-art ultra-low-voltage LSs. The table is divided into two sections: the first one refers to measurements on the fabricated prototypes, while the second section is related to the comparison with only simulated previously proposed circuits. The LS proposed in [7] and fabricated using a 0.35 μm process exhibits relatively low standby power consumption at the expense of very long delay and high energy per transition. Among the LSs realized in the 0.18 µm technology node, the one presented in [4] results to be the most energy hungry. On the other hand, the design proposed in [14] exhibits the lowest energy consumed per transition at expense of a minimum up-convertible V_{DDL} of only 0.21 V. As shown above, the proposed circuit reliably extends the operating voltage conversion range down to 0.1 V, while consuming 2.6 times less static power than the circuit proposed in [14] and decreasing the silicon area of about 30%. Fabricated circuits in more advanced technology nodes are not directly comparable with our proposal. However, as specified in Section II, the two most recent LSs [11, 12] were replicated in the adopted 0.18 μm CMOS process. To further extend our comparison analysis, three additional recent proposals [10, 15, 16], designed with the same technology node and evaluated for the same operating conditions, were also considered. From results of the second portion in Table II, it can be observed that the LS proposed by *Matsuzuka et al.* [15] represents the fastest solution. From simulated delay (24.5 ns) reported in Section II, the proposed LS is only 13% slower but it results extremely competitive exhibiting a power consumption (both static and dynamic) by far lower than that of all its counterparts as well as the widest conversion range.

IV. CONCLUSION

In this paper, we presented an energy-efficient DCVS-based level shifter which can up-convert from the deep subthreshold regime to the nominal supply voltage of 1.8V. The proposed design was fabricated in the 180nm UMC technology process and validated through experimental measurements. Obtained results demonstrate that the proposed circuit can convert an input signal as low as 96 mV (on average) to 1.8 V. Moreover, when converting a 400 mV input to 1.8 V, it exhibits an average propagation delay of 31.7 ns and an energy per transition of 93 fJ. This is obtained while consuming an average static power of less than 60 pW and occupying only 108.8 µm^2.

REFERENCES

[1] V. Kursum, E.G. Friedman, "Supply and Threshold Voltage Scaling Techniques" In *Multi-Voltage CMOS Circuit Design*, John Wiley & Sons, Ltd, pp. 45–84, 2006.

[2] B. Zhai *et al.*, "Energy-efficient subthreshold processor design," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 8, pp. 1127–1137, Aug. 2009.

[3] K. Craig. Y. Shakhsheer, S. Arrabi, S. Khanna, J. Lach, and B. H. Calhoun, "A 32 b 90 nm processor implementing panoptic DVS achieving energy efficient operation from sub-threshold to high performance," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 545–552, Feb. 2014.

[4] H. Shao and C.-Y. Tsui, "A robust, input voltage adaptive and low energy consumption level converter for sub-threshold logic," *In Proc. of ESSCIRC 2007*, pp. 312–315, Sep. 2007.

[5] S. Lütkemeier, U. Rückert, "A Subthreshold to Above-Threshold Level Shifter Comprising a Wilson Current Mirror", *IEEE Trans. Circuits Systems II*, vol. 57, no. 9, pp. 721-724, Sept. 2010.

[6] S. N. Wooters, B. H. Calhoun, and T. N. Blalock, "An energy-efficient subthreshold level converter in 130-nm CMOS," *IEEE Trans. Circuits Systems II*, vol. 57, no. 4, pp. 570–578, Apr. 2010.

[7] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "A low-power level shifter with logic error correction circuit for extremely low-voltage digital CMOS LSIs," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 1776–1783, Jul. 2012.

[8] M. Lanuzza, P. Corsonello and S. Perri, "Low-Power Level Shifter for Multi-Supply Voltage Designs," *IEEE Trans. on Circuits and Systems II*, vol. 59, no. 12, pp. 922-926, Dec. 2012.

[9] Y. Kim, Y. Lee, D. Sylvester, and D. Blaauw, "SLC: Split-control level converter for dense and stable wide-range voltage conversion," *in Proc. of ESSCIRC 2012*, pp. 478–481, Sep. 2012.

[10] S.R. Hosseini, M. Saberi, R. Lotfi, "A Low-Power Subthreshold to Above-Threshold Voltage Level Shifter," *IEEE Trans. Circuits Systems II*, vol. 61, no. 10, pp. 753-757, Oct. 2014.

[11] S.-C. Luo, C.-J. Huang and Y.-H. Chu,"A wide-range level shifter using a modified wilson current mirror hybrid buffer," *IEEE Trans. Circuits Systems I*, vol. 61, no. 6, pp. 1656-1665, 2014.

[12] W. Zhao, A. Alvarez, Y. Ha, "A 65-nm 25.1-ns 30.7-fJ Robust Subthreshold Level Shifter with Wide Conversion Range", *IEEE Trans. Circuits Systems II*, vol. 62, no. 7, pp. 671–675, Jul. 2015.

[13] M. Lanuzza, P. Corsonello, S. Perri, "Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23 , no. 2, pp. 388-391, Feb. 2015.

[14] J. Zhou, C. Wang, X. Liu, *X.* Zhang, M. Je, "An ultra-low voltage level shifter using revised wilson current mirror for fast and energy-efficient wide-range voltage conversion from sub-threshold to I/O voltage," *IEEE Trans. Circuits Systems I*, vol. 62, pp. 697–706, Mar. 2015.

[15] R. Matsuzuka, T. Hirose, Y. Shizuku, N. Kuroki, M. Numa, "A 0.19-V Minimum Input Low Energy Level Shifter for Extremely Low-Voltage

VLSIs", Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, pp. 2948 - 2951, 24-27 May 2015.

[16] S. R. Hosseini, M. Saberi, R. Lotfi, "An Energy-Efficient Level Shifter for Low-Power Applications", ", Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, pp. 2241 - 2244, 24-27 May 2015.

[17] M. Lanuzza, S. Strangio, F. Crupi, P. Palestri, and D. Esseni, "Mixed Tunnel-FET/MOSFET Level Shifters: a new proposal to extend the Tunnel-FET application domain," *IEEE Trans. on Electron Devices*, vol. 62, no. 12, pp. 3973 - 3979, Dec. 2015. ~~to be published.~~

[18] F. Ishihara, F. Sheikh, and B. Nikolic, "Level conversion for dual-supply systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 2, pp. 185–195, Feb. 2004.