Threshold Voltage Instability in p-GaN Gate AlGaN/GaN HFETs

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***Abstract*—We investigate the impact of the gate contact on the threshold voltage stability in p-GaN gate AlGaN/GaN HFETs with double pulse measurements on p-GaN gate devices and with device simulations. We find that, under gate stress, in the case of high-leakage Schottky contact to the p-GaN gate a negative threshold voltage shift results from hole accumulation in the p-GaN region. Conversely, in the case of low-leakage Schottky contact, hole depletion in the p-GaN region gives rise to a positive threshold voltage shift. More generally, we show that an imbalance between the hole tunnelling current through the Schottky barrier and the thermionic current across the AlGaN barrier results in a variation of the total charge stored in the p-GaN region, which in turn is responsible for the observed threshold voltage shift. Finally, we present a simplified equivalent circuit model for the p-GaN gate module.**

***Index Terms*—HEMT, p-GaN gate, Schottky contact, threshold voltage shift, gate stress, hole injection.**

I. Introduction

ENHANCEMENT-mode operation is a highly desirable feature in power electronics applications. Normally-off GaN-based heterojunction field effect transistors (HFETs) can be obtained by growing a p-GaN gate on an AlGaN/GaN heterojunction [1], [2], [3], as shown in Fig. 1. Threshold voltage exceeding 1 V is achievable with such a device concept [4], [5]. However, due to the intrinsic p-n junction formed by the p-GaN gate and the electron channel, a large input current can result as the gate voltage approaches the diode built-in potential, that is around 3.4 V. Thus, the gate voltage overdrive and, consequently, the maximum output current have to be limited in order to contain driver losses. However, this can compromise the switching speed and the device on-resistance.

A Schottky contact at the p-GaN gate can be used to reduce the gate current by several orders of magnitude [6], [7]. However, as the leakage is reduced, the p-GaN region becomes floating, and unstable operation can result when charge is accumulated in the p-GaN during device operation [8], [9]. Indeed, threshold voltage instabilities have a critical impact on device operation. Negative threshold voltage shifts can induce spurious turn-on and undermine safe operation. Positive threshold voltage shifts, on the other hand, can negatively impact the device on-resistance and the switching times.

Device reliability is also deeply affected by the gate module concept [10], [11], [12]. Floating holes can move under applied voltage during device operation and locally modify the electric fields, deeply impacting reliability [13]. In addition, the gate module failure mechanism drastically changes as the gate current is reduced by means of a Schottky contact. In the ohmic case, under gate stress conditions, current is allowed to flow through the gate junction and, as in common p-n diodes, thermal runaway is responsible for device breakdown. In low-leakage Schottky gate devices, instead, the reverse biased Schottky junction must withstand a high electric field under gate stress conditions, and gate breakdown might occur due to the formation of stress-induced percolation paths, as in insulated-gate devices [14], [15], [16].

In this paper we investigate the impact of the gate contact on the threshold voltage stability. An ohmic gate and a Schottky gate p-GaN HFET have been fabricated. The two gate module concepts have been analysed and compared by means of double-pulse gate stress measurements and extensive device simulations. The main results of our investigation can be summarised as follows:

1) A variation in the total (hole) charge in the p-GaN results in a threshold voltage shift, negative if holes are accumulated, positive if the p-GaN is depleted of holes. Therefore, the threshold voltage depends on the balance between the inflow of holes from the Schottky contact, and the outflow of holes through the p-n junction.
2) A high-leakage Schottky-contact p-GaN gate suffers from negative threshold-voltage shift after gate stress, due to hole accumulation in the p-GaN region.
3) Low-leakage Schottky-contact devices are prone to positive threshold-voltage shift after gate stress, due to hole depletion in the p-GaN.
4) Hole accumulation at the channel/back-barrier interface results in a negative threshold voltage shift.

II. Fabricated Devices and Measurements

Two p-GaN-gate HFETs have been fabricated, one with a nearly ohmic gate contact, the other with a Schottky gate contact. The device structure is sketched in Fig. 1. The ohmic contact was made with Ti [17], whereas TiN was used for the Schottky contact. The magnesium concentration in the p-GaN is around $9\times10^{19}\,\mathrm{cm}^{-3}$, and the hole density is estimated to be around $10^{18}\,\mathrm{cm}^{-3}$. The typical threshold voltage, measured as the gate voltage at $I_{\mathrm{DS}} = 10\,\mu$A/mm and $V_{\mathrm{DS}} = 0.5$ V, is 1 V. The channel electron density and mobility are $6 \times 10^{12}\,\mathrm{cm}^{-2}$ and $1500\,\mathrm{cm}^2/(\mathrm{V{\cdot}s})$, respectively.

The measured gate currents for the two devices are shown in Fig. 2. A suppression of the input leakage of four orders of magnitude is achieved with the Schottky contact. The Schottky

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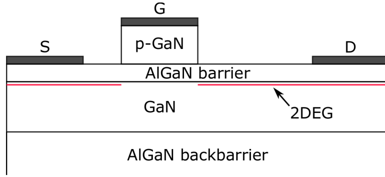

Fig. 1. Schematic device structure of the fabricated p-GaN gate AlGaN/GaN HFETs.

barrier height is estimated to be 1.5 eV for the ohmic contact and 2.5 eV for the Schottky contact [17], [18].

The Ti contact shows a slightly rectifying behaviour, but in the following it will be referred to as the ohmic-contact case.

In order to assess the threshold voltage stability for the two gate module concepts, double-pulse gate stress experiments have been performed. In particular, pulsed transfer characteristics for different gate stress voltages have been extracted [9]. In this experiment, the gate was stressed with a positive voltage (base line), and the samples of the transfer characteristic were extracted periodically, i. e., the device was periodically switched between a stress phase and a measurement phase. The stress phase duration was 1 ms, whereas the measurement phase duration was 1 μs. The transfer characteristic was sampled from 0 V to 5 V, with a step of 0.1 V. That is, the gate voltage in the measuring phase was periodically increased by 0.1 V, from 0 V to 5 V. The drain electrode was kept at 0 V during stress, and switched to 0.5 V in the measuring phase. Finally, the drain current was recorded at the end of each measurement phase, in order to obtain the transfer characteristic. In Figs. 3 and 4, the threshold voltage shift as a function of the gate base voltage is shown for the ohmic and the Schottky contact, respectively. The gate stress voltage in the ohmic case has been intentionally limited to 4 V, in order to keep the maximum gate current below 1 mA/mm and, consequently, at a comparable level with the Schottky gate case. As can be seen, in the case of the ohmic contact $\Delta V_{\rm th}$ is always negative, and increases with increasing gate stress voltage. Instead, in the case of Schottky gate contact the threshold voltage shift has a non monotonic trend with the applied gate stress: it is negative for $V_{\rm GS} \leq 5$ V, positive for higher gate base voltages.

III. Device Simulations

We have performed two-dimensional drift-diffusion simulations of a normally-off p-GaN gate HFET [19]. The considered structure is depicted in Fig. 1, and include a 100-nm-thick p-GaN layer on a 10-nm-thick $Al_{0.2}Ga_{0.8}N$ barrier. Incomplete ionization of magnesium acceptors has been taken into account with a ionization energy of 170 meV. The magnesium acceptor concentration is 10^{20} cm^{-3}, resulting in a hole density of about 10^{18} cm^{-3}. The electron and hole low-field mobility are $1500\,\mathrm{cm^2/(V{\cdot}s)}$ and $10\,\mathrm{cm^2/(V{\cdot}s)}$, respectively. The spontaneous and piezoelectric polarization have been accounted for according to the model described in [19], [20]. Surface donors have been included at the SiN/AlGaN interface as to give a channel electron density of 6×10^{12} cm^{-2}. The hole tunnelling mass is $0.6\cdot m_0$ (m_0 is the electron mass at rest). The influence

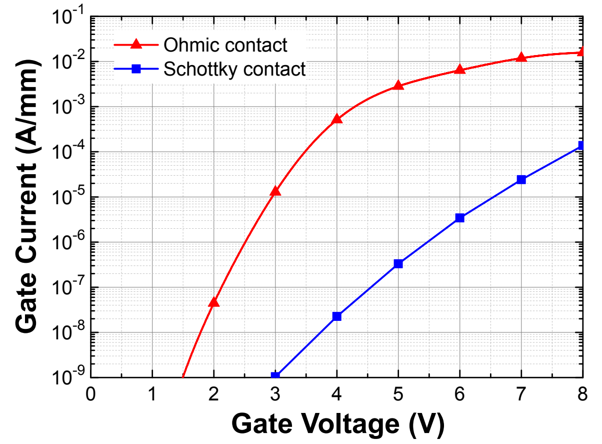

Fig. 2. Measured gate current as a function of the gate voltage for the ohmic and the Schottky gate contact cases at room temperature.

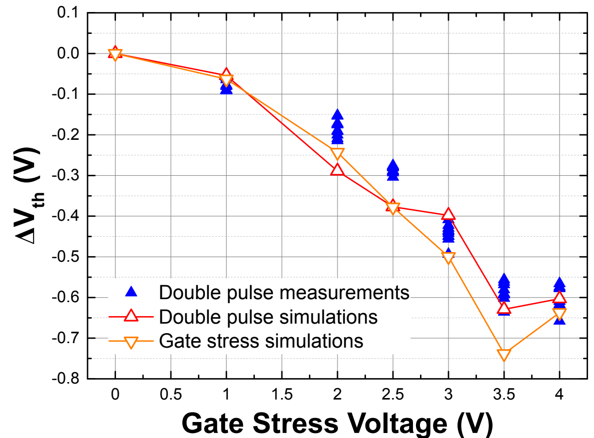

Fig. 3. Measured and simulated threshold voltage shift as a function of the gate base voltage extracted from double-pulse transfer characteristics for the ohmic gate contact. In blue triangles, double pulse measurements. Solid red line and up triangles, complete double pulse simulations. Solid orange line and down triangles, simplified gate stress simulations for $t_{\rm stress} = 1$ s

of an $Al_{0.05}Ga_{0.95}N$ back-barrier [21], placed 150 nm away from the barrier/channel interface, was also considered.

The pulsed transfer characteristics as a function of the gate base voltage have been reproduced via detailed transient simulations. The extracted threshold voltage shift as a function of the gate stress voltage is compared with the experimental data in Figs. 3 and 4. Each point corresponds to double-pulse transfer characteristic simulation. A remarkable agreement between measurements and simulation is obtained, meaning that the dominant physical mechanisms underlying the observed threshold voltage shifts are captured by our simplified model.

IV. Gate Stress Simulations

Since detailed double-pulse transient simulations are time consuming and the interpretation of the output is not self-evident, simplified gate stress simulations have also been performed, in order to obtain a systematic physical interpretation of the $V_{\rm th}$ variations under gate stress conditions. In particular, we consider the following gate stress simulation: a gate voltage pulse is applied for a time $t_{\rm stress}$, then the gate voltage is set to

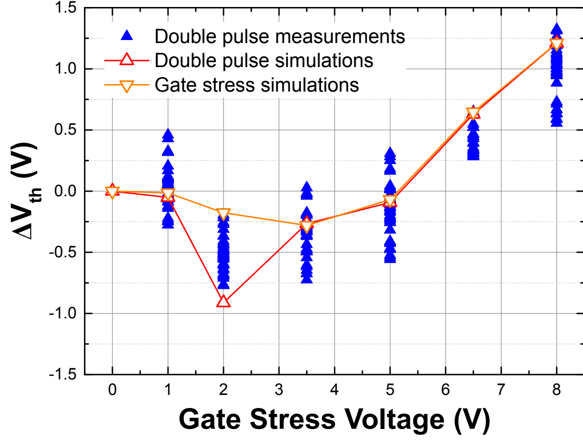

Fig. 4. Measured and simulated threshold voltage shift as a function of the gate base voltage extracted from double-pulse transfer characteristics for the Schottky gate contact. In blue triangles, double pulse measurements. Solid red line and up triangles, complete double pulse simulations. Solid orange line and down triangles, simplified gate stress simulations for $t_{\text{stress}} = 1\,\text{s}$

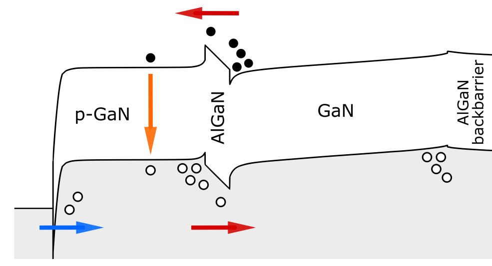

Fig. 5. Sketch of the band diagram along a vertical cut under the p-GaN gate for $V_{\text{GS}} > 0\,\text{V}$, in the general case of tunnelling Schottky gate contact. The mechanisms responsible for the threshold voltage shift are shown. Blue arrow, hole tunnelling through the Schottky barrier; red arrows, thermionic emission across the AlGaN barrier; yellow arrow, carrier recombination in the p-GaN. Hole accumulation at channel/back-barrier interface is also sketched.

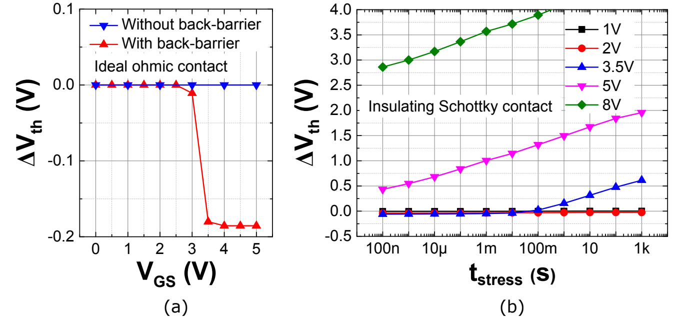

Fig. 6. (a) Threshold voltage shift after a 1 s gate stress phase as a function of the applied gate stress voltage for the ideal ohmic contact case. (b) Threshold voltage shift as a function of the applied gate stress duration for $V_{\text{GS}} = 5\,\text{V}$ in the case of insulating Schottky contact.

zero and after 100 ns the threshold voltage shift is evaluated. In order to not perturb the state of the system, the threshold voltage variation has been calculated as follows. First, the variation of the surface potential ψ_{s} [22] at the channel/barrier interface under the p-GaN gate with respect to the situation before stress is extracted. Then, the threshold voltage shift is calculated as

$$\Delta V_{\text{th}} = -\Delta\psi_{\text{s}} \left(\left. \frac{d\psi_{\text{s}}}{dV_{\text{G}}} \right|_{V_{\text{G}}=0} \right)^{-1}, \quad (1)$$

where the derivative of the surface potential with respect to the gate voltage is extracted from simulations before stress. This method allows the threshold voltage shift induced by a gate voltage stress to be sampled and represented as a function of the stress amplitude and duration. Furthermore, in this way the state of the system is not altered by the V_{th} extraction procedure, as it would be if the threshold voltage was extracted from a DC transfer characteristic simulation.

For $t_{\text{stress}} \geq 1\,\text{ms}$, the ΔV_{th} extracted with this method approaches that from a complete double-pulse simulation. This is demonstrated in Figs. 3 and 4, where the simplified gate stress simulations for $t_{\text{stress}} = 1\,\text{s}$ are compared with the complete double pulse simulations.

In the following, we shall discuss two idealised cases: the ideal ohmic contact and the perfectly insulating Schottky contact. Then, the more general Schottky contact including tunnelling will be investigated.

A. *Ideal Ohmic Contact*

In this case, ohmic boundary conditions are imposed at the gate contact. We shall use this simple case to investigate the impact of hole injection in the GaN buffer and of the AlGaN back-barrier on the threshold voltage.

The p-GaN region forms with the underlying electron channel a p-n junction with an intrinsic built-in potential around the GaN band-gap. When the gate voltage exceeds this potential the p-n junction becomes forward biased and hole injection in the GaN buffer, as well as electron injection in the p-GaN, take place, as sketched in Fig. 5. Charge neutrality in the GaN channel is restored by the electrons coming from the source, giving rise to conductivity modulation [2].

As can be seen in Fig. 6(a), if no back-barrier is present, after a gate stress voltage is applied, no threshold voltage shift is observed if electrons and holes are allowed to recombine. The minority carrier injection has just an impact on turn-off time, as in conventional p-n diodes.

When an AlGaN back-barrier is introduced the equilibrium threshold voltage is shifted to the right by the negative polarization charge at the channel/back-barrier interface [21].

As depicted in Fig. 5, when the gate diode is forward biased, injected holes from the p-GaN are moved by the vertical electric field towards the channel/back-barrier interface, and the negative polarization charge is screened by the resulting hole distribution. This gives rise to a negative threshold voltage shift that acts to counterbalance the static positive shift introduced by the back-barrier polarization charge. However, the electron and hole distributions are spatially separated, and even if the gate voltage is removed, the injected holes are confined in the GaN buffer by the vertical electric field and can not recombine with electrons. Hence, the effective recombination time for accumulated holes in the back-barrier can be extremely long, resulting in an almost permanent ΔV_{th}.

In Fig. 6(a), the threshold voltage shift after a 1 s gate stress pulse is applied as a function of the gate stress voltage. Only

radiative recombination is considered in the simulation. The $V_{\rm th}$ shift is always negative and saturates to a value dependent on carrier lifetime, which decreases in absolute value with increasing recombination rates, as can be easily verified by simulations. As can be seen, the shift is correlated with the gate diode turn-on, when holes start to be injected into the device.

In summary, with an AlGaN back-barrier, an almost permanent but finite negative threshold voltage shift results from accumulation of injected holes at the channel/back-barrier interface.

B. Insulating Schottky Contact

In principle, the DC gate current can be suppressed by insulating the p-GaN region with a reverse-biased Schottky contact. In this case, holes are confined in the floating p-GaN region by the Schottky barrier from one side, and by the AlGaN barrier from the other (Fig. 5). The p-GaN is capacitively coupled with the gate electrode and, as long as the p-n gate diode is off, the variations of its potential are determined by the capacitive voltage divider formed by the Schottky junction depletion capacitance and the capacitance between the p-GaN and the source and drain contacts. When a positive gate stress voltage is applied such that the p-GaN electric potential exceeds the p-n diode forward bias voltage, electrons are injected in the p-GaN and holes leak in the GaN channel via thermionic emission through the AlGaN barrier, as sketched in Fig. 5. Injected electrons in the p-GaN can either recombine with holes or exit from the gate contact, depending on their diffusion length and on p-GaN thickness. Therefore, by either injection in the GaN channel or via recombination with injected electrons, the p-GaN is depleted of holes, i.e., the floating p-GaN region is negatively charged by the forward-biased p-n diode. Now, a larger gate voltage is needed to push the required amount of holes against the p-GaN/AlGaN interface to form the electron channel, that is, hole depletion in the p-GaN results in a positive threshold voltage shift.

In Fig. 6(b), the threshold voltage shift after a gate stress is shown as a function of the stress amplitude and duration. When the gate voltage is applied, holes are removed at the edge of the Schottky contact depletion region (the depletion region widens) and accumulate at the p-GaN/AlGaN interface. If the resulting p-GaN electric potential is smaller than the diode forward voltage ($V_{\rm GS} \lesssim 3.4\,{\rm V}$) the threshold voltage remains constant. If the resulting p-GaN electric potential exceeds the diode forward voltage, the p-n junction discharges the p-GaN region, and the threshold voltage increases. In this case, the p-GaN potential is roughly clamped to the p-n junction forward voltage, and the remaining $V_{\rm GS}$ drops entirely across the Schottky depletion region, so that the negative charge is stored entirely as depletion charge in the Schottky junction. So the larger is the gate stress voltage the larger is the accumulated negative charge and the $\Delta V_{\rm th}$. More precisely, as the p-GaN is discharged, the p-n junction bias voltage decreases with time, so that the threshold voltage shift increases logarithmically with the applied stress time. The process is irreversible as holes cannot be supplied by any contact, and the total hole quantity in the p-GaN can only decrease. Therefore, a floating p-GaN gate results in unstable device operation.

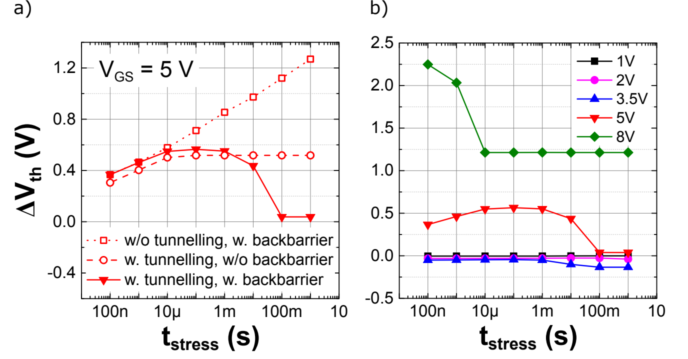

Fig. 7. (a) Threshold voltage shift as a function of the applied gate stress time for $\phi_{\rm B} = 2.8\,{\rm eV}$ and $V_{\rm GS} = 5\,{\rm V}$. In dashed line, with hole tunnelling, without back-barrier. In solid line, with hole tunnelling, with back-barrier. In dotted line, without hole tunnelling, with back-barrier. (b) Threshold voltage shift as a function of the applied gate stress duration and voltage for a tunnelling Schottky contact with $\phi_{\rm B} = 2.8\,{\rm eV}$.

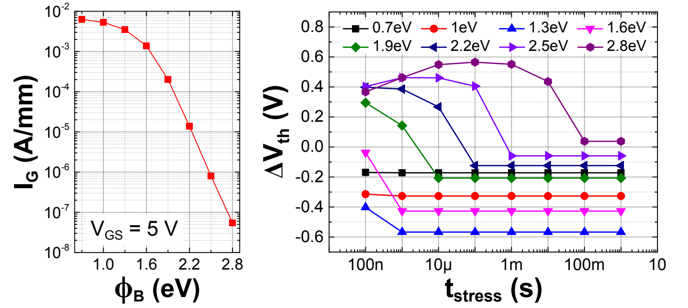

Fig. 8. (Left) Gate current as a function of the Schottky barrier height for $V_{\rm GS} = 5\,{\rm V}$. (Right) Threshold voltage shift as a function of the applied gate stress duration and Schottky barrier height, for $V_{\rm GS} = 5\,{\rm V}$.

In summary, in the case of insulating Schottky contact a positive gate voltage stress results in a permanent positive threshold-voltage shift due to negative net charge in the p-GaN gate.

C. General Schottky Contact

The two cases previously considered represent limiting cases of a more general Schottky contact, where the transmission probability of holes through the Schottky barrier is non-zero and finite.

In Fig. 7, the evolution of the threshold voltage after a gate stress pulse is applied is shown. A Schottky barrier of $2.8\,{\rm eV}$ and hole tunnelling mass of $0.6{\cdot}m_0$ are assumed, that result in a rather small gate current of approximately $50\,{\rm nA/mm}$ at $5\,{\rm V}$. In Fig. 7(a), the tunnelling and the insulating contact case are compared for $V_{\rm GS} = 5\,{\rm V}$. For such $V_{\rm GS}$, the resulting p-GaN to source voltage is sufficient to turn on the p-n junction, and hole depletion in the p-GaN occurs, giving rise to a positive $\Delta V_{\rm th}$. Up to $10\,\mu{\rm s}$ after the gate stress is applied, the threshold voltage evolves exactly as in the insulated case. As the p-GaN is discharged, its electric potential decreases, and consequently the current through the p-n junction diminishes. Then, without AlGaN back-barrier, steady-state is reached when the p-n

junction current is balanced by the hole tunnelling current, and $\Delta V_{\rm th}$ saturates. With the AlGaN back-barrier, thanks to the additional negative shift due to hole accumulation at the channel/back-barrier interface, the threshold voltage shows almost full recovery of its initial value. As can be seen in Fig. 7(b), when the stress voltage is increased to $8\,$V, the threshold voltage shows a considerable quasi-permanent positive shift.

As already stated, negative charging due to hole depletion in the p-GaN results in a positive threshold voltage shift. By the same reasoning, an excess of holes results in a negative shift of the threshold voltage. If the applied gate stress amplitude is such that the resulting p-GaN potential is lower than the p-n diode forward voltage (Fig. 7(b)), holes can be injected in the p-GaN via tunnelling through the Schottky barrier and accumulate at the p-GaN/barrier interface without leaking across the AlGaN barrier. If the input voltage is rapidly removed, as in our simulation, the tunnelling probability through the Schottky barrier decreases considerably, as the electric field at the contact/p-GaN interface decreases, and the excess holes are stuck in the p-GaN, giving rise to a negative threshold voltage shift. This mechanism has already been reported by [8]. The time required to restore equilibrium conditions, i.e., for holes to leave the p-GaN region by tunnelling, depends on the gate current, and increases as the leakage is reduced. This behaviour can be observed in Fig. 7(b) for $V_{\rm GS} = 3.5\,$V. The p-GaN is slowly charged by the hole tunnelling current, resulting in a negative threshold voltage shift after $10\,$ms.

In Fig. 8, the $\Delta V_{\rm th}$ dependence on the gate leakage current is shown. In our numerical experiment we have chosen the Schottky barrier height as the independent variable to modulate the gate current. In Fig. 8(a) the dependence of the gate leakage at $V_{\rm GS} = 5\,$V on ϕ_B is shown, whereas in Fig. 8(b) the threshold voltage evolution for different values of the barrier height is shown. If, in order to reduce the driving current, the gate leakage is reduced below $\sim 1\,$mA/mm at $5\,$V (Fig. 8), that is ϕ_B is larger than $1.6\,$eV, a negative $\Delta V_{\rm th}$ is observed. In this gate current range, an excess of holes builds up in the p-GaN during the stress phase. When the gate voltage is brought to zero to sense the threshold voltage, the accumulated holes are confined in the p-GaN by the Schottky barrier and a negative shift of the threshold voltage is registered. If we further decrease the gate current, $\Delta V_{\rm th}$ becomes positive. In this case, the p-GaN is depleted by the p-n diode, as the hole tunnelling current is smaller than the current through the p-n junction. Then the $V_{\rm th}$ shift tends to saturate as the tunnelling current starts to balance the current through the p-n junction. Finally, the threshold voltage decreases due to the holes accumulating in the GaN buffer. The lower is the gate current the lower is the hole injection rate in the GaN channel, so that as the Schottky barrier height increases the positive threshold voltage overshoot transient gets longer.

We can now give a physical interpretation of the double pulse experiments. In the nearly ohmic gate case shown in Fig. 3, during the stress phase, the large inflow of holes from the contact results in an excess of positive charge in the p-GaN. Due to the fast switching time, the charge can not be completely removed, and a negative threshold-voltage shift appears. In the Schottky-gate case shown in Fig. 4, hole accumulation in the p-GaN occurs as long as the p-n diode is off, i.e. for $V_{\rm GS} < 5\,$V, so that $\Delta V_{\rm th} < 0\,$V. For $V_{\rm GS} > 5\,$V, the p-n junction turns on, and the hole inflow from the Schottky contact is not sufficient to balance the outflow from the p-n junction. Therefore, the p-GaN is depleted and negative charge is stored during the stress phase, resulting in a $\Delta V_{\rm th} > 0\,$V.

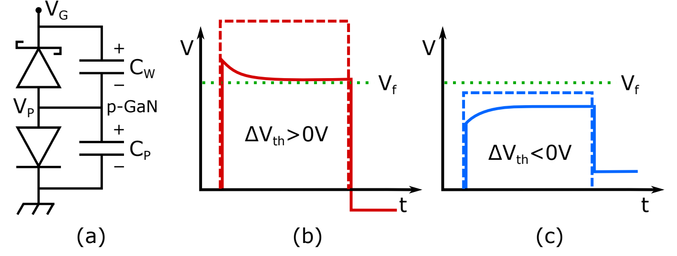

Fig. 9. (a) Equivalent circuit of the p-GaN gate module. (b)-(c) Gate stress voltage transient in the equivalent circuit. (b) The initial $V_{\rm P}$ exceeds V_f and $\Delta V_{\rm th} > 0\,$V. (c) The initial $V_{\rm P}$ is smaller than V_f and $\Delta V_{\rm th}$ is negative. In dashed lines $V_{\rm G}$, in solid lines $V_{\rm P}$.

V. Equivalent Circuit

In Fig. 9(a), the equivalent circuit of the p-GaN gate module is shown, assuming the source and the drain terminals grounded. The p-GaN/channel junction is modelled as an ideal p-n diode with a non-linear capacitance $C_{\rm P}$ in parallel, whereas the Schottky gate contact is represented as the parallel of a leaky Schottky diode (the diode is conducting under reverse bias due to tunnelling through the Schottky barrier) and the depletion capacitance $C_{\rm W}$. $C_{\rm P}$ is equal to the gate capacitance of the same device but with an ideal ohmic contact.

As shown in Fig. 9(b), when a positive gate voltage step is applied, the initial p-GaN potential $V_{\rm P}$ is determined by non-linear capacitive voltage divider composed of $C_{\rm W}$ and $C_{\rm P}$, whereas its steady-state value depends on the non-linear voltage divider of the two diodes. If the initial $V_{\rm P}$ is lower than the p-n diode forward voltage V_f, the p-GaN node is positively charged by the current through the Schottky diode and $V_{\rm P}$ rises. When the gate voltage is removed the p-GaN is left with a positive charge and a positive voltage, i.e., a negative $\Delta V_{\rm th}$. If the initial $V_{\rm P}$ is larger than V_f, the p-n diode turns on and clamps $V_{\rm P}$ to V_f. Hence, the charge accumulated on $C_{\rm P}$ is roughly independent of the gate voltage, whereas the charge on $C_{\rm W}$ depends on the difference $V_{\rm G} - V_f$. Therefore, a negative charge accumulates in the p-GaN node. In this case, when the gate voltage is removed, $V_{\rm P}$ is brought to a negative value by the capacitive voltage divider, and the accumulated negative charge is stored.

The threshold voltage shift $\Delta V_{\rm th}$ can be expressed as a function of the total charge Q stored in the p-GaN node as follows:

$$\Delta V_{\rm th} \approx -\frac{Q}{C_{\rm W}(0)}, \qquad (2)$$

where $C_{\rm W}(0)$ is the differential capacitance of the Schottky contact at equilibrium, obtained as $C_{\rm W}(0) = -dQ_{\rm W}/dV_{\rm W}|_{V_{\rm W}=0}$, being $Q_{\rm W}$ the depletion charge at the

Schottky contact, and V_{W} the potential difference across the capacitor C_{W} (Fig. 9).

VI. Conclusion

Threshold voltage instabilities in p-GaN gate HFETs have been investigated by means of double pulse measurements on fabricated devices with different gate contact, i.e. ohmic vs Schottky, and comparison with device simulations. We have shown that the threshold voltage depends on the balance between the hole tunnelling current through the Schottky barrier, and the thermionic current across the AlGaN barrier, that can result in a variation of the total charge stored in the p-GaN, and ultimately in a threshold voltage shift. Thus, with a high leakage Schottky contact, a negative threshold voltage shift is observed, whereas a positive variation of the threshold voltage occurs with a low-leakage Schottky contact. The impact of an AlGaN back-barrier has been investigated, and we have shown that an almost permanent but finite negative threshold voltage shift appears due to hole accumulation at the channel/back-barrier interface. Finally, an equivalent circuit model for the p-GaN gate module has been presented and discussed.

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