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Comparative evaluation of analogue front-end designs for the CMS Inner Tracker at the High Luminosity LHC

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Comparative evaluation of analogue front-end designs for the CMS Inner Tracker at the High Luminosity LHC

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Abstract: The CMS Inner Tracker, made of silicon pixel modules, will be entirely replaced prior to the start of the High Luminosity LHC period. One of the crucial components of the new Inner Tracker system is the readout chip, being developed by the RD53 Collaboration, and in particular its analogue front-end, which receives the signal from the sensor and digitizes it. Three different analogue front-ends (Synchronous, Linear, and Differential) were designed and implemented in the RD53A demonstrator chip. A dedicated evaluation program was carried out to select the most suitable design to build a radiation tolerant pixel detector able to sustain high particle rates with high efficiency and a small fraction of spurious pixel hits. The test results showed that all three analogue front-ends presented strong points, but also limitations. The Differential front-end demonstrated very low noise, but the threshold tuning became problematic after irradiation. Moreover, a saturation in the preamplifier feedback loop affected the return of the signal to baseline and thus increased the dead time. The Synchronous front-end showed very good timing performance, but also higher noise. For the Linear front-end all of the parameters were within specification, although this design had the largest time walk. This limitation was addressed and mitigated in an improved design. The analysis of the advantages and disadvantages of the three front-ends in the context of the CMS Inner Tracker operation requirements led to the selection of the improved design Linear front-end for integration in the final CMS readout chip.

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Contents

1   CMS pixel detector upgrade for the High Luminosity LHC

The High Luminosity upgrade [1] of the CERN Large Hadron Collider (LHC) [2] will boost its potential for physics discoveries, but also impose extreme operating conditions for the experiments. Along with the accelerator, the Compact Muon Solenoid (CMS) [3] detector will be substantially upgraded during Long Shutdown 3, starting in 2025 [4]. This upgrade is referred to as the CMS Phase-2 Upgrade [5]. The silicon tracking system, located at the heart of CMS, detects trajectories of charged particles. It will be entirely replaced during the Long Shutdown 3 because of the accumulated radiation damage and to take advantage of the increased luminosity. The goal of the upgrade is to maintain or improve the tracking and vertex reconstruction performance of the detector in the harsh environment of the High Luminosity LHC (HL-LHC). The CMS Phase-2 tracker will consist of the Outer Tracker, made of silicon modules with strip and macro-pixel sensors, and the Inner Tracker (IT), based on silicon pixel modules [6].

The high granularity of the IT offers excellent spatial resolution, which is important for a precise three-dimensional reconstruction of particle trajectories, as well as the identification of primary interaction vertices and secondary decay vertices. One quarter of the latest layout of the Phase-2 IT in the r-z[1] view is shown in figure 1. The IT will consist of a barrel component with four

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[1]CMS adopts a right-handed coordinate system with the origin centred at the nominal collision point inside the experiment. The x axis points towards the centre of the LHC, the y axis points vertically upwards and the z axis points along the beam direction. The azimuthal angle ϕ is measured from the x axis in the x-y plane, the radial coordinate in this plane is denoted by r and the polar angle θ is measured from the z axis. The pseudorapidity η is defined as $\eta = -\ln\tan(\theta/2)$ [6].
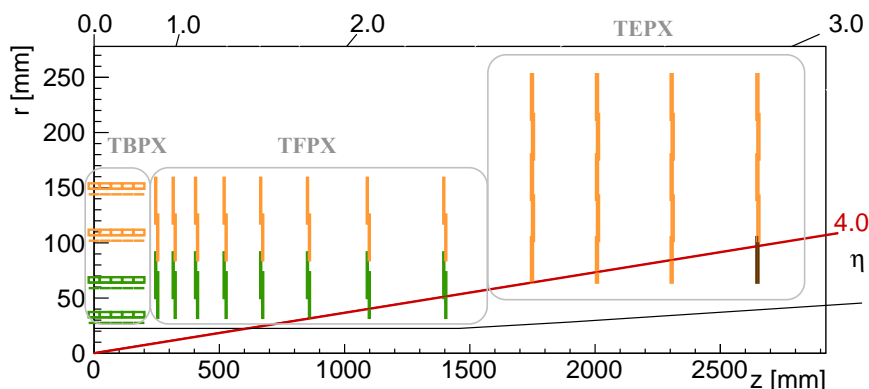
Figure 1. Layout of one quarter of the Phase-2 Inner Tracker in the *r*-*z* view. Green lines correspond to pixel modules with two readout chips and orange lines represent modules with four chips. The modules shown in brown correspond to the innermost ring of the last TEPX disc ($z = 2650$ mm), which will be used by the Beam Radiation Instrumentation and Luminosity (BRIL) project [7] for dedicated luminosity and background measurements. The grey line represents the beam pipe envelope.

cylindrical layers, referred to as the Tracker Barrel Pixel detector (TBPX). Eight smaller double-discs forming the Tracker Forward Pixel detector (TFPX) and four larger double-discs forming the Tracker Endcap Pixel detector (TEPX) will be placed in the forward direction on each side. The forward acceptance will be extended up to a pseudorapidity of $|\eta| = 4$ [6], as indicated by the red line in figure 1.

The IT detector will have an active area of 4.9 m^2 and it will be composed of 3892 pixel modules. Two pixel sizes are currently being considered for the Phase-2 IT: $100 \times 25\,\mu\text{m}^2$ pixels and $50 \times 50\,\mu\text{m}^2$ pixels. With a pixel size of $2500\,\mu\text{m}^2$ there would be about 2 billion readout channels. The detector design strives for a minimal mass of the detector to avoid degradation of the tracking performance due to the interactions of particles with the detector material. Therefore, lightweight mechanical structures made of carbon fiber, two-phase CO_2 cooling [6] and a low voltage powering scheme based on serial powering [8] will be used. The data will be transmitted through low-mass electrical links and optical fibers [6] to further reduce the detector mass.

The main building block of the IT system is a hybrid pixel module, shown in figure 2. It is composed of a silicon sensor bump-bonded to two or four readout chips. Pixel modules with two readout chips are indicated in green in figure 1 and modules with four chips are indicated in orange. The readout chips of the module are wire-bonded to a flexible printed circuit board with passive components and connectors, called the high density interconnect, that distributes power (low voltage to power the pixel chips and high voltage to bias the sensor), clock and control signals and collects data from the chips. Signals produced in the sensor are transmitted to the front-end electronics, where they are processed and the data are stored during the planned 12.8 µs trigger latency interval. The hit information is sent to the back-end data acquisition system of the experiment only after receipt of a Level-1 trigger [9] signal. In the innermost layer of the IT, the hit rate will reach $3.5\,\text{GHz}\,\text{cm}^{-2}$, while the CMS Level-1 accept rate will increase from 100 to 750 kHz [9].
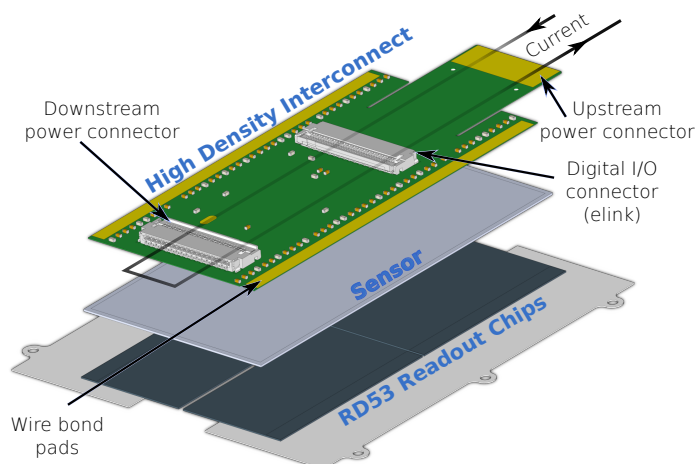
Figure 2. A 3D exploded view of the Phase-2 Inner Tracker pixel module with four readout chips [10]. From top to bottom the following components can be seen: the high density interconnect, the silicon pixel sensor, the RD53 readout chips, and the rails to mount the module on a support structure and to ensure the electrical isolation of the module.
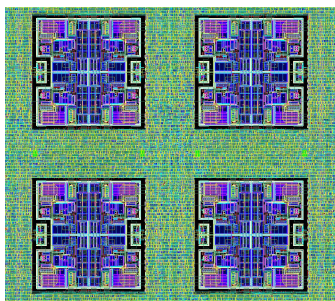
2   RD53A analogue front-ends

A high-performance radiation tolerant pixel readout chip is essential for good tracking performance of the IT operating during the HL-LHC era. Such a readout chip is being designed in TSMC [11] 65 nm CMOS technology by the RD53 Collaboration [12], a joint effort between the ATLAS and CMS experiments. A large-scale demonstrator chip called RD53A [13] containing design variations was produced. Its purpose is to demonstrate the suitability of the chosen technology for low threshold, low noise, and low power operation at high hit rates, to verify sufficient radiation tolerance [14], and to select the most suitable design for the final readout chip. It is a mixed signal chip, having both analogue and digital circuits. It features custom-designed intellectual property blocks, such as clock data recovery and phase locked loop blocks [15] for the clock recovery from the command stream running at 160 Mb/s; a high speed output transmitter with a current mode logic cable driver [16] sending data at 1.28 Gb/s on up to four output lanes; and a shunt low-dropout regulator [17] for serial powering of the pixel modules. The chip size is 20.0×11.8 mm^2, which is about half the size of the final chip, as it shares the chip reticle with CMS Outer Tracker chips. The pixel matrix is composed of 400×192 square pixels with 50 µm pitch. All the common analogue and digital circuitry needed to bias, configure, monitor, and read out the chip is placed at the bottom chip periphery [13].

The analogue-to-digital conversion is performed by the analogue front-end (AFE), whose basic structure (shown in figure 3) includes a charge sensitive amplifier (CSA), usually referred to as preamplifier (PA), a feedback circuit taking care of the signal return to baseline and leakage current compensation, a threshold discriminator, a threshold trimming circuit to address pixel-to-pixel variation of the threshold voltage, and a time-over-threshold (TOT) counting of the input signal amplitude. In the RD53A chip the TOT$_{40}$ digitization with 4-bit resolution is done with respect to rising edges of the 40 MHz LHC clock.[2] Therefore, one TOT$_{40}$ unit corresponds to 25 ns [13]. The chip also features

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[2]In the final pixel chip, the counting will be performed on both the rising and the falling edge of the clock, resulting in a finer TOT$_{80}$ counting at 80 MHz with one TOT$_{80}$ unit equal to 12.5 ns [18].
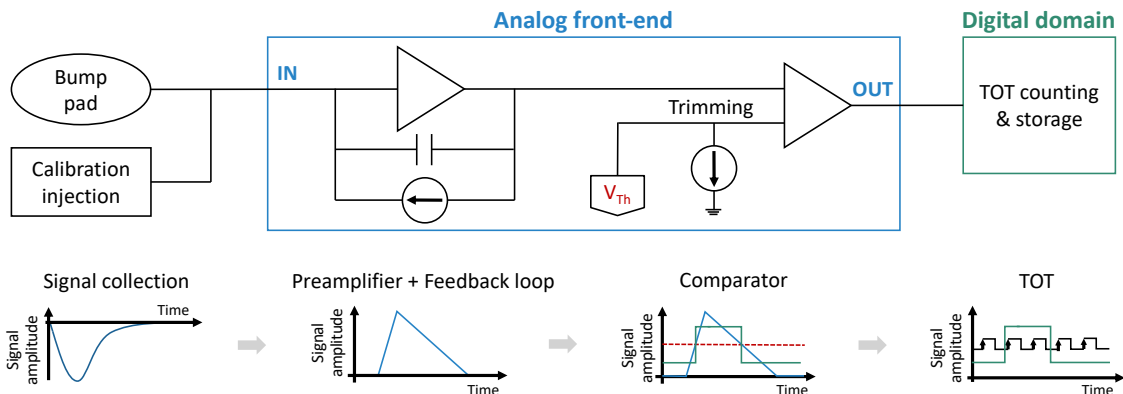
Figure 3. Signal processing steps in different stages of a generic analogue front-end, from signal collection to digitization.

Figure 4. RD53A layout of four analogue islands, i.e. sixteen pixels, surrounded by the fully synthesized digital "sea" [13].
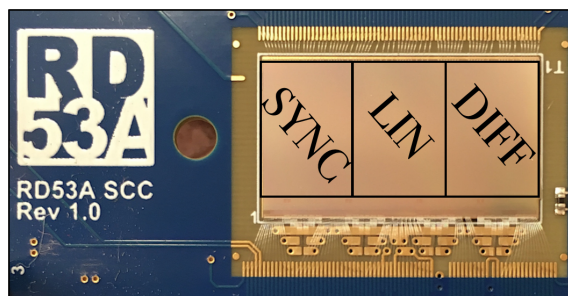
Figure 5. Photograph of the RD53A chip, wire-bonded to a test card, indicating the placement of the three analogue front-ends.

a circuit for the generation of internal calibration charge injection signals. The circuit, connected to the input of the PA, enables the injection of a well-defined and programmable charge to test the front-end functionalities and calibrate the chip response. Every pixel in the RD53A chip contains the same circuit based on two switches that generate voltage steps fed to an injection capacitor [13].

The RD53A AFEs are grouped by four, i.e. 2×2 pixels, into analogue "islands", which are embedded in a synthesized digital "sea", as shown in figure 4. Three different AFE designs have been proposed within the RD53 project to explore different options for the ATLAS and CMS experiments leaving open the possibility that the experiments might make different choices. The chip is divided horizontally into three sections, each one having one AFE design, as indicated in figure 5. The synchronous (SYNC) AFE is implemented between columns 0 and 127, the linear (LIN) AFE between columns 128 and 263, and the differential (DIFF) AFE between columns 264 and 399. It was not possible to have an equal area for all three designs because the 400-pixels wide matrix is built of 8×8 pixel cores [13]. The three AFEs share the digital logic and the chip periphery in the RD53A chip [13]. All three AFEs are based on a CSA with a feedback loop ensuring the return to baseline of the PA output after each hit. The gain of the PA can be chosen globally thanks to different feedback capacitors (C_F) present in each AFE. The specific features of each AFE are discussed in the following paragraphs.
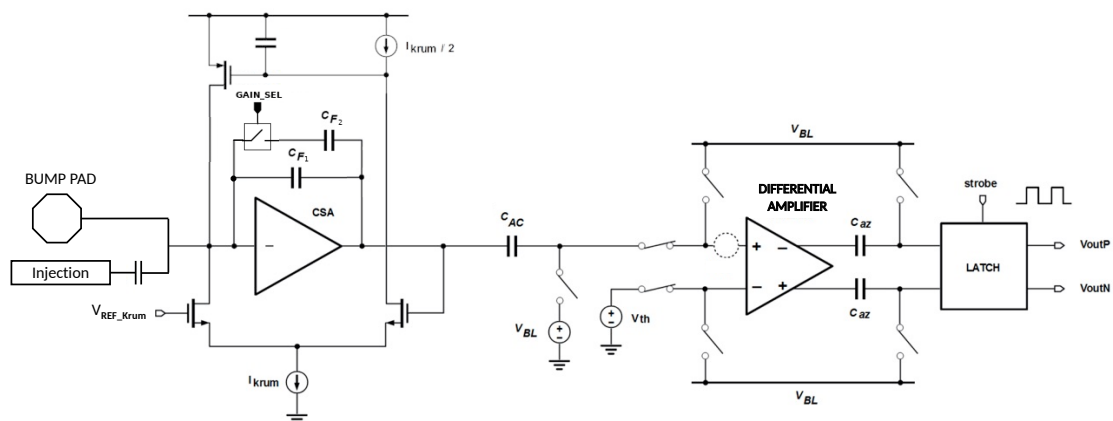
Synchronous front-end. The schematic of the Synchronous front-end is shown in figure 6. It features a single-stage CSA with a Krummenacher feedback (I_{Krum}, V_{REF_Krum}) [19], which ensures both the sensor leakage current compensation and the constant current discharge of the feedback capacitor. The Krummenacher current (I_{Krum}) drives the speed of the PA output return to baseline. The PA is AC-coupled (C_{AC}) to a synchronous discriminator composed of a differential amplifier, providing a further small gain, and a positive feedback latch, which performs the signal comparison with a threshold (V_{th}) and generates the discriminator output. The latter can also be switched to a local oscillator with a selectable frequency higher than the standard LHC clock, in order to perform a fast TOT counting. The distinctive feature of this AFE is a so-called "auto-zero" functionality. In traditional designs, the transistor mismatch causing pixel-to-pixel variations of the threshold is compensated with a trimming digital-to-analogue converter (DAC). In the SYNC AFE instead, internal capacitors (C_{az}) are used to compensate voltage offsets automatically. A periodic acquisition of a baseline (V_{BL}) is required, which can be done during LHC abort gaps [13, 20].
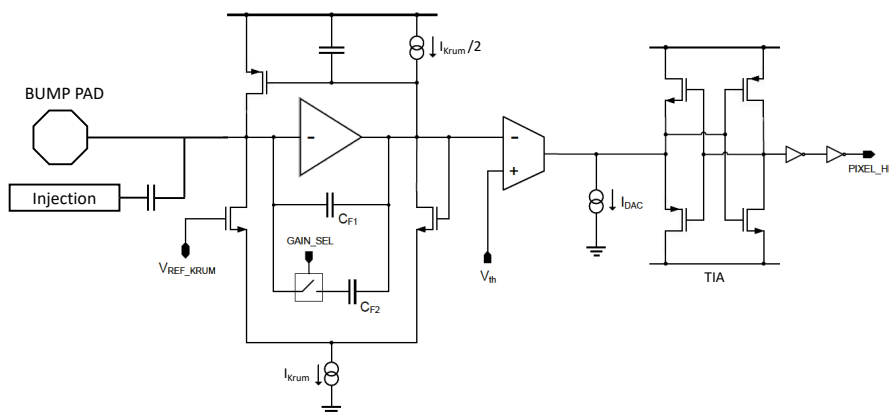
Linear front-end. The Linear front-end implements a linear pulse amplification in front of the discriminator. The schematic of this AFE is shown in figure 7. As for the SYNC AFE, the PA of the LIN AFE is based on a CSA featuring a Krummenacher feedback (I_{Krum}, V_{REF_Krum}). The signal from the CSA is fed to a low power threshold discriminator based on current comparison, which compares the signal with the threshold (V_{th}). It is composed of a transconductance stage followed by a transimpedance amplifier (TIA) providing a low impedance path for fast switching. A 4-bit binary weighted trimming DAC with adjustable range (I_{DAC}) allows for a reduction in the threshold dispersion across the pixel matrix [13, 21].

Differential front-end. The PA of the Differential front-end, shown in figure 8, has a continuous reset (I_{ff}), unlike the other two designs, which use the Krummenacher feedback with constant current reset. This continuous feedback is able to prevent the input from saturation for a leakage current of up to 2 nA [18]. For higher currents, a dedicated leakage current compensation (LCC) circuit can be enabled. The LCC is disconnected from the input when disabled, which improves the AFE stability and noise performance. The DC-coupled precomparator provides additional gain in front of the comparator and acts as a differential threshold circuit, i.e. the global threshold is adjustable through two distributed threshold voltages (V_{th1} and V_{th2}) instead of one. The precomparator stage is followed by a classic time-continuous comparator. The threshold is trimmed in each pixel using a local 5-bit trimming DAC (TDAC) [13].

The basic functionalities of the RD53A chip and each of the three AFEs were previously verified and reported [22–26]. The objective of this work was to evaluate the three AFE designs against the CMS requirements, in terms of spurious hit rate, dead time, and radiation tolerance and to compare their performance. A dedicated evaluation program was established and the most relevant detector performance parameters were studied. The key measurements that enabled CMS to identify the most suitable option for integration into the CMS pixel detector are presented in this paper. All presented test results were obtained with the BDAQ53 test system [27], using the calibration injection circuit, with RD53A chips bump-bonded to sensors with rectangular pixels, i.e. $100 \times 25\,\mu m^2$, if not

Figure 6. Schematic of the Synchronous front-end implemented in the RD53A chip [13].

Figure 7. Schematic of the Linear front-end implemented in the RD53A chip [13].
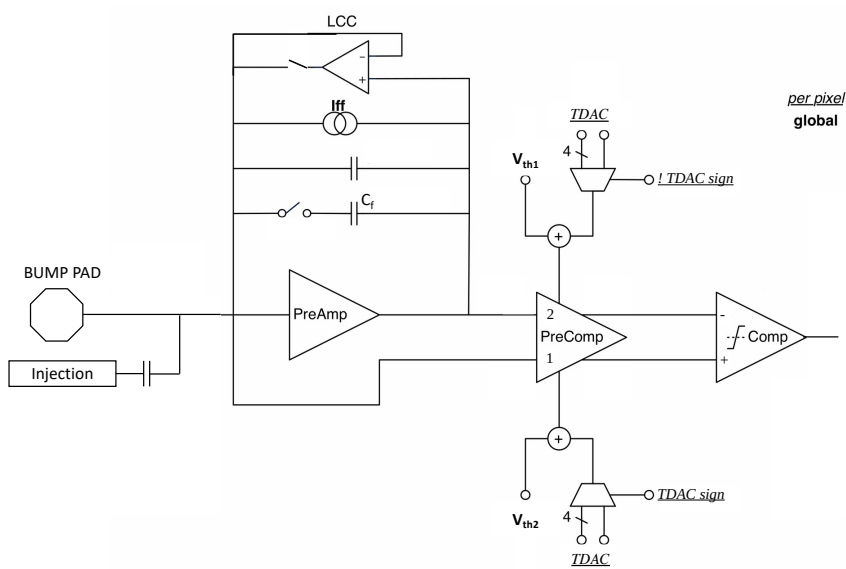
Figure 8. Schematic of the Differential front-end implemented in the RD53A chip [13].

otherwise stated, and operated at cold temperature (T ≈ −10 °C), which is the lowest temperature that could be achieved with the cooling systems available for the lab setups.

3   CMS requirements for the analogue front-end

The first step towards the choice of the AFE for the CMS final chip was the establishment of the evaluation criteria. The most relevant detector parameters were used to derive the following CMS requirements:

Optimal threshold. The new CMS readout chip will feature $50 \times 50\,\mu m^2$ pixels, while the pixel size is $100 \times 150\,\mu m^2$ in the present CMS pixel detector [28]. The readout chip can be bump-bonded either to sensors with square pixels of the same size or to rectangular pixels of $100 \times 25\,\mu m^2$, thanks to electrode routing in the sensor [6]. Silicon sensors with a thickness of $150\,\mu m$ will be used. This is about half the thickness of the current $285\,\mu m$ thick sensors [28]. The main advantage of thin sensors is better radiation tolerance, but the collected signal charge is smaller. The charge distribution obtained with $120\,GeV$ protons from a test beam collected in a $130\,\mu m$ thick sensor with $100 \times 150\,\mu m^2$ pixels is shown in figure 9. The most probable value (MPV) is about $7900\,e^-$ before irradiation. While this number is about 10% lower than the expectation, it is well compatible with it within the measurement uncertainties (e.g. due to the charge calibration). The MPV decreases by about $2000\,e^-$ after irradiation to $1.2 \times 10^{15}\,n_{eq}/cm^2$ [6]. Based on the expected signal, a detection threshold of $1000\,e^-$ is required by CMS for the innermost layer of the IT to ensure sufficient detection efficiency, especially with irradiated sensors. A threshold of $1200\,e^-$ is sufficient for the outer layers of the detector, where the fluence is lower.

The number of pixels hit increases with the incidence angle of the particle, giving clusters with large hit multiplicity in particular in the high-η part of the barrel. In this specific part of the detector, the charge collection path in a pixel is similar to the pixel dimension in the z direction, hence $\gtrsim 50\,\mu m$ for square pixels and $\gtrsim 100\,\mu m$ for rectangular pixels, to be compared with a charge collection path of $150\,\mu m$ at normal incidence. For this reason, in the high-η region of the barrel square pixels are disfavoured, being more prone to remain below threshold, notably after irradiation.
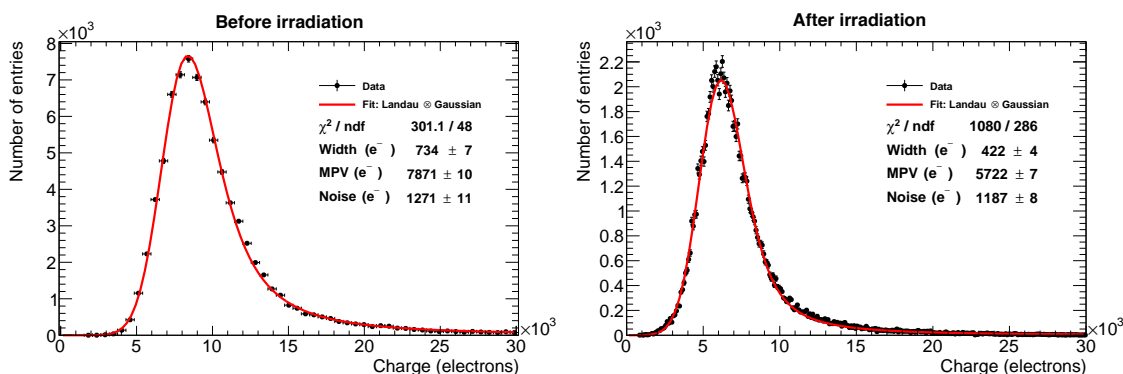

Figure 9. Test beam measurement of the collected charge before (left) and after (right) irradiation to $1.2 \times 10^{15}\,n_{eq}/cm^2$, using single pixel clusters, in a $130\,\mu m$ thick pixel sensor with $100 \times 150\,\mu m^2$ pixels. The red line represents a fit to a Landau distribution convoluted with a Gaussian [6].

Radiation tolerance. The IT is the CMS subdetector closest to the LHC interaction point and therefore it is exposed to the highest radiation levels. Two scenarios are envisaged for the HL-LHC: in the "nominal" scenario, the accelerator would deliver a maximum of 140 proton-proton (pp) collisions per bunch crossing, to reach a total integrated luminosity of $3000\,\mathrm{fb}^{-1}$ by the end of the physics program. In the "ultimate" scenario, the number of pp collisions per bunch crossing would be pushed up to 200, reaching an integrated luminosity of $4000\,\mathrm{fb}^{-1}$. A fluence reaching $2.6 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$ and a total ionizing dose (TID) up to $1.4\,\mathrm{Grad}$ are expected in the innermost layer in the nominal scenario, while the figures would scale up to $3.4 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$ and $1.9\,\mathrm{Grad}$ in the ultimate scenario. The RD53A chip was designed to withstand a TID of at least $500\,\mathrm{Mrad}$ and an average leakage current up to $10\,\mathrm{nA/pixel}$ [14]. However, with this specification the radiation levels expected in CMS, reaching $1.9\,\mathrm{Grad}$ in the ultimate luminosity scenario, would imply a replacement of the innermost layer of the IT barrel after every two years of operation. The CMS Collaboration aims for a single replacement of the innermost layer during the ten-year lifetime of the detector, hence a higher radiation tolerance is necessary.

Noise occupancy. For a stable operation at low threshold it is important to minimize the front-end noise to have an acceptable fraction of spurious hits in the data. Single pixels that are too noisy can be disabled, to keep the overall noise occupancy low, but their fraction must be low in order not to significantly affect the detector efficiency. Based on the occupancy simulation for different parts of the detector, shown in figure 10, the average noise occupancy of the new front-end is required to be below 10^{-6}, i.e. two orders of magnitude below the lowest expected occupancy.

Dead time. CMS requires a maximum dead time of 1% in the innermost layer of the IT barrel to ensure high detection efficiency even at the highest expected hit rate. This requirement translates to a maximum efficiency loss of 1% at maximum hit rate caused by the total dead time (digital + analogue). The dead time in the RD53A chip has a minor contribution from the digital buffering and
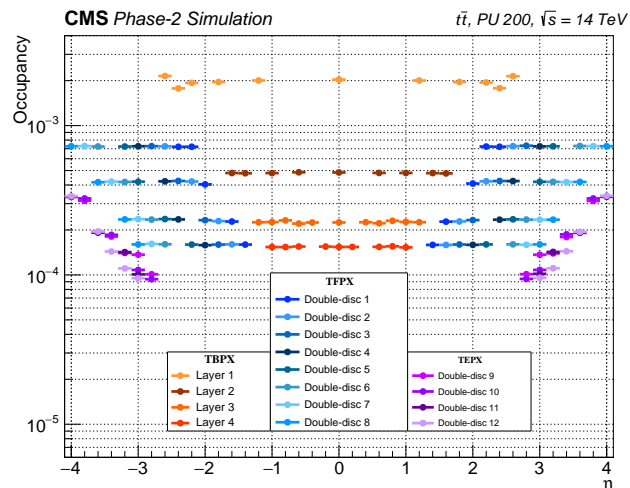

Figure 10. Simulation of the hit occupancy as a function of pseudorapidity for all layers and double-discs of the IT for simulated top quark pair production events with a pileup of 200 events [6].

a major contribution from the CSA of the AFE. While the digital contribution is due to the limited hit buffer size and cannot be reduced with the chip settings, the AFE dead time depends on the TOT response calibration. The TOT response to a given input charge can be set in the chip to a certain number of TOT_{40} units (one TOT_{40} unit corresponds to one 40 MHz clock cycle, i.e. to 25 ns). The charge resolution is obtained by dividing the input charge by the corresponding number of clock cycles and can therefore be expressed in e^-/TOT_{40} units.

A Monte Carlo simulation of hit efficiency losses due to the digital, analogue, and total dead time is shown in figure 11 for two charge resolutions: 1500 e^-/TOT_{40} and 3000 e^-/TOT_{40}. The simulation was performed for two pixel module positions in the innermost layer of the IT barrel: the centre ($z = 0$), denoted L1c, and the edge, denoted L1e. For each position, both pixel geometries were simulated. The rectangular pixels are represented with solid bins and the square pixels with hashed bins. The square pixels have a slightly higher inefficiency. As expected, the TOT charge resolution has no influence on the digital dead time, and the hit losses caused by the AFE are smaller with the coarser charge resolution of 3000 e^-/TOT_{40}. The efficiency losses are higher in the centre making the dead time requirement difficult to meet. With the charge resolution of 1500 e^-/TOT_{40} the requirement is not satisfied in any of the two module positions, while with 3000 e^-/TOT_{40} the requirement is satisfied on average. The hit efficiency losses are slightly above the requirement in the centre and slightly below at the edge. The charge resolution of 3000 e^-/TOT_{40} was therefore taken as the TOT calibration requirement for the AFE evaluation.

The impact of charge resolution on tracking performance was also evaluated. Simulation of the tracking performance for the reconstruction of single muons with a transverse momentum of 10 GeV was performed with planar 150 μm-thick sensors, with both sensor pixel geometries and two different thresholds: 1200 e^- and 2400 e^-. The resolution on the transverse (d_0) and longitudinal (z_0) impact parameters, denoted $\sigma(d_0)$ and $\sigma(z_0)$ respectively, integrated over the full η range are shown in fig-
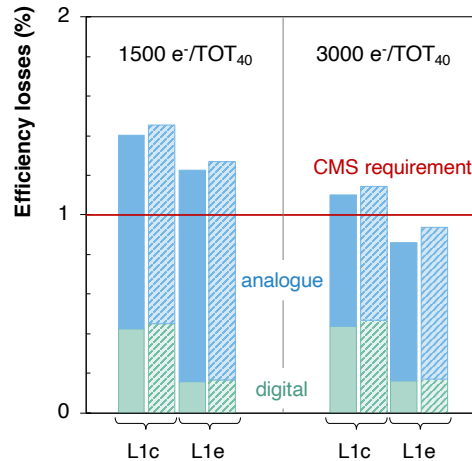
Figure 11. Hit efficiency losses due to the digital buffering (green) and analogue dead time (blue) simulated in the 200 pileup scenario for two charge resolutions: 1500 e^-/TOT_{40} and 3000 e^-/TOT_{40}. The simulation was done for the centre (c) and edge (e) of the innermost layer (L1) of the IT barrel and for two pixel geometries: the solid bins represent the $100 \times 25\,\mu m^2$ pixels and hashed bins represent the $50 \times 50\,\mu m^2$ pixels. The red line represents the CMS requirement.

ure 12 for three charge resolutions: $600\,e^-/TOT_{40}$, $3000\,e^-/TOT_{40}$ and $6000\,e^-/TOT_{40}$. The impact parameter resolution deteriorates for a higher threshold and appears to be insensitive to the charge resolution. Since a higher charge resolution does not affect the tracking performance, a charge resolution of $3000\,e^-/TOT_{40}$ was taken as the baseline calibration for the inner regions of the Inner Tracker.
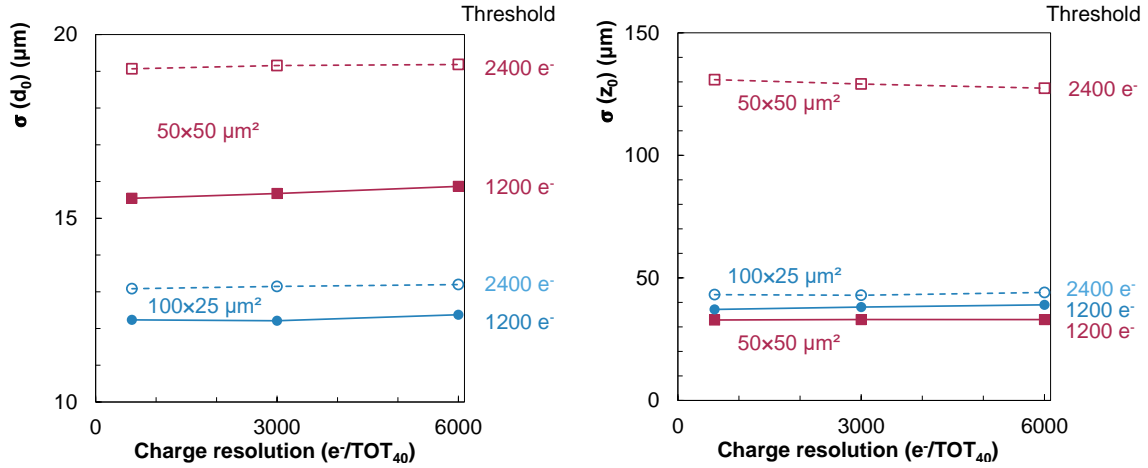

Figure 12. Influence of the charge resolution on the transverse (left) and longitudinal (right) impact parameter resolution obtained from simulation. The $100 \times 25\,\mu m^2$ pixels are represented in blue and the $50 \times 50\,\mu m^2$ pixels are represented in red. The full markers and solid lines indicate the threshold of $1200\,e^-$ and the open markers and dashed lines indicate the threshold of $2400\,e^-$.

4 Equalization of threshold dispersion

The calibration injection circuit is used to inject a range of charges to measure the threshold of each pixel and the threshold dispersion across the matrix. The occupancy versus charge of a pixel is a sigmoid from 0 to 100% occupancy, commonly called an S-curve. An example of an S-curve plot including more than 26 000 pixels is shown in figure 13(a). The calibration charge at which 50% occupancy is reached is taken as a measurement of the charge equivalent of the threshold of each pixel. The mean value of the pixel threshold distribution represents the global threshold and the root-mean-square (RMS) is the threshold dispersion. Typically, pixel-to-pixel variations result in a threshold dispersion of several hundred electrons, which can be reduced to less than hundred electrons after setting optimal trim bits for each pixel with a dedicated tuning algorithm. Examples of untuned and tuned threshold distributions are shown in figure 13(b) and figure 13(c), respectively.

The threshold tuning capability of the three AFE designs was tested and proven to be functional in many samples, some of which were irradiated and re-evaluated afterwards. An assembly of an RD53A chip and a sensor with $50 \times 50\,\mu m^2$ pixels was irradiated at Karlsruhe Institute of Technology [29] with 23 MeV protons up to a fluence of $3 \times 10^{15}\,n_{eq}/cm^2$, corresponding to a TID reaching 350 Mrad. The RD53A chip was not powered during irradiation. The sample was irradiated at room temperature and maintained at cold temperature after irradiation to avoid annealing. It was tested at $-10\,°C$ in a dry environment. The sensor bias voltage was adjusted to reach an average leakage current of $10\,nA/pixel$, which is the maximum specified value for the RD53A chip [14]. The pixels with a noise occupancy higher than 10^{-4} were considered noisy and masked, based on

(a) S-curves.

(b) Untuned threshold distribution.
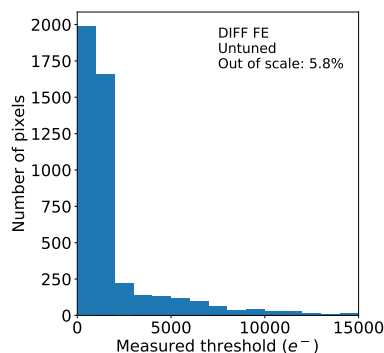
(c) Tuned threshold distribution.
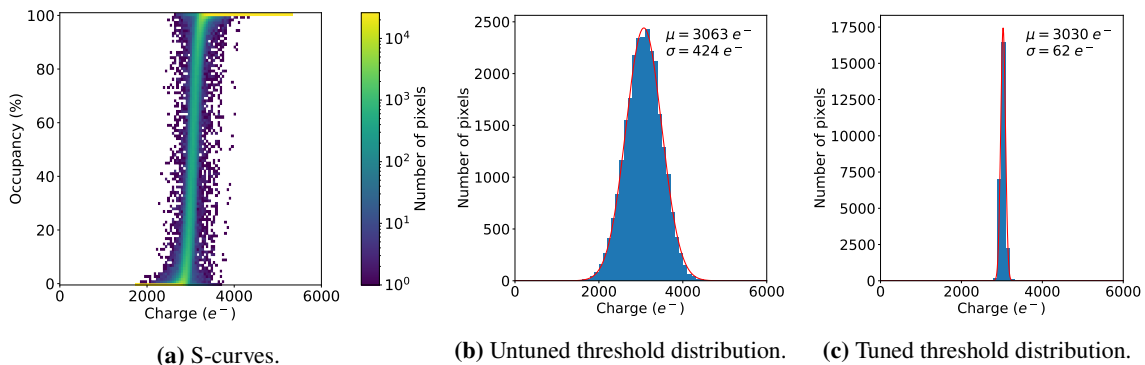
Figure 13. S-curves (a) and threshold distribution before (b) and after (c) tuning obtained with all pixels of the LIN AFE of one RD53A chip. The red lines in the threshold distributions represent fits to Gaussian distributions and the mean (μ) and width (σ) of the fit functions are given.

(a) SYNC AFE.
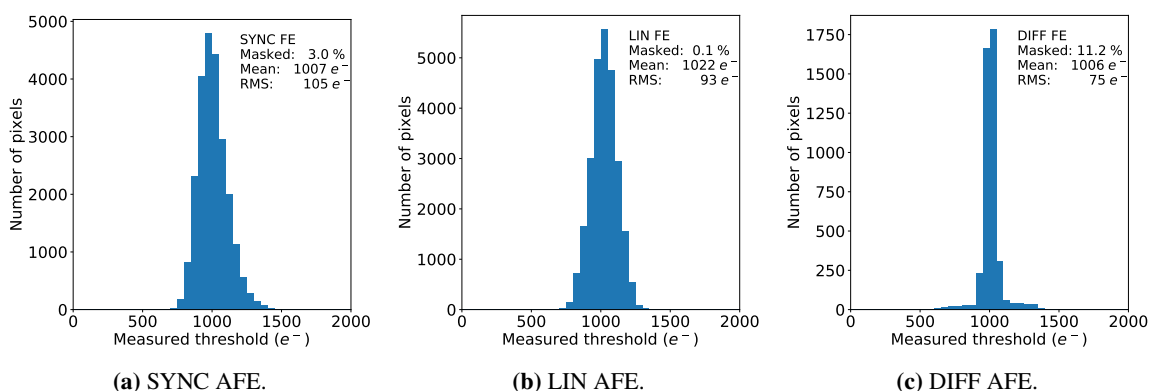
(b) LIN AFE.

(c) DIFF AFE.

Figure 14. Threshold distributions of the SYNC AFE (a), the LIN AFE (b), and the DIFF AFE (c) obtained with an RD53A chip after irradiation. The mean and RMS were calculated using all non-masked pixels in each AFE.

the lowest hit occupancy expected from the simulation presented in figure 10. The remaining pixels were tuned to a threshold of 1000 e$^-$. Pixels with an anomalously high threshold that could not be adjusted with the range of the trim bits were masked in the tuning procedure. The threshold distributions of the three AFEs after tuning are shown in figure 14.

All three AFEs were functional after irradiation and could reach the required threshold with a threshold dispersion of about 100 e$^-$. The threshold tuning of the LIN AFE worked well and only 0.1% of pixels were masked. The auto-zeroing in the SYNC AFE worked well too, however the leakage current caused a higher noise in this front-end and 3% of the pixels were masked. The threshold distribution of the DIFF AFE features a narrow core and long tails, and 11.2% of pixels were masked. The large fraction of masked pixels in the DIFF AFE is the consequence of a long tail in the untuned threshold distribution, shown in figure 15. Pixels with a too high threshold cannot be tuned to the desired threshold value because the range covered by the trim bits is a global setting for the whole chip. As the threshold dispersion depends on several AFE parameters, many parameter combinations were tried to mitigate the problem, and the 11.2% of masked pixels was the best result that could be achieved with this irradiated sample.

Figure 15. Untuned threshold distribution of the DIFF AFE in the irradiated RD53A chip.

This study triggered an investigation and the design team discovered that the combined effect of irradiation and cold temperature resulted in a PMOS threshold increase in the DIFF precomparator, resulting in a small voltage margin. Simulations showed that the voltage margin is smaller at cold temperature and decreases with irradiation, reaching a value close to zero for the DIFF AFE design implemented in the RD53A chip after irradiation to 200 Mrad, which explains the problematic threshold tuning observed after irradiation to 350 Mrad. A design improvement of the DIFF precomparator was proposed and simulated, obtaining an extension of the expected operation range up to 500 Mrad, although this radiation level is still low compared to the dose expected in the CMS detector. With such operation range, replacements of the innermost layer would be required every two years once the ultimate luminosity is reached, while CMS is aiming at a single replacement during the whole high-luminosity program. For this reason the attention turned to the other two AFEs, which seem promising candidates for a higher radiation tolerance.

5 Noise evaluation

The evaluation of the noise levels in the RD53A chip was done by sending triggers, without any charge injection, so that each recorded hit was induced by the noise. The average noise occupancy is then defined as the number of noise hits per pixel and per trigger. It was measured for the three AFEs, using a non-irradiated RD53A chip with a sensor with the highest capacitance, i.e. rectangular pixels, operated at a temperature of about $-10\,^\circ\mathrm{C}$. Single noisy pixels can be disabled to reduce the rate of noise hits. However, the fraction of disabled pixels should not significantly increase the detection inefficiency. A single pixel was considered noisy if its noise occupancy was above 10^{-4} based on the lowest occupancy expected in the IT detector from simulation (figure 10). Therefore, as a first step of the noise evaluation, every pixel with more than 100 hits in 10^6 triggers was disabled at a threshold of 1200 e$^-$. As a second step, a new set of 10^6 triggers was sent to each front-end to measure the noise occupancy of the non-masked pixels. In case of very low noise more triggers were sent. Results of noise occupancy measurements are presented in figure 16. The fraction of masked noisy pixels is indicated in the legend and the maximum noise occupancy of 10^{-6}, required by CMS, is indicated by the red line. The TOT was calibrated to 1100 e$^-$/TOT$_{40}$.

First, the influence of the threshold on the average noise occupancy was evaluated. The result is shown in figure 16(a). The threshold was gradually decreased from 1200 e$^-$, keeping the same
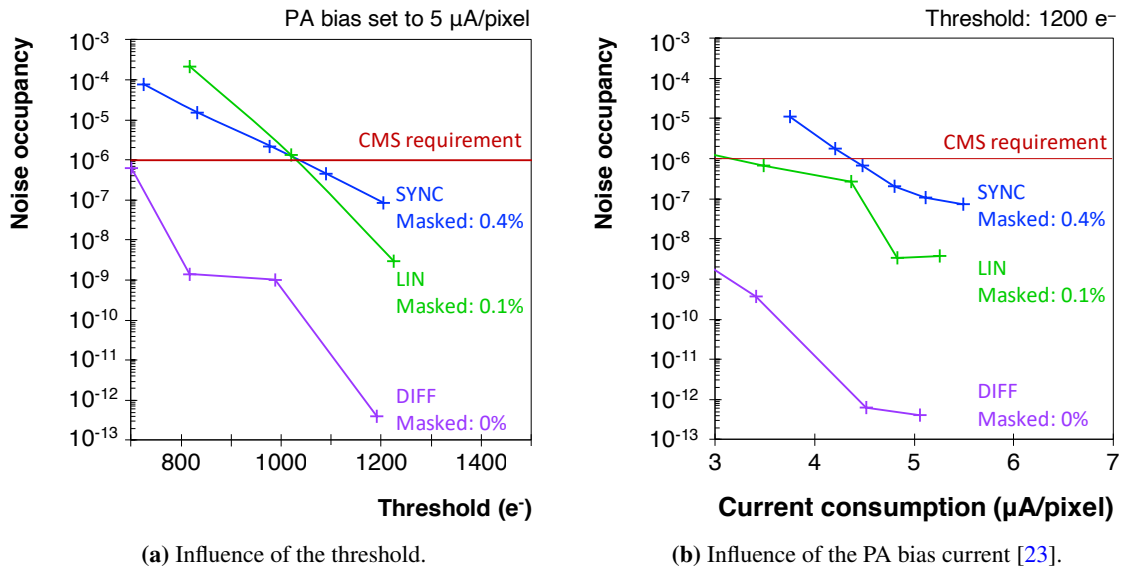
Figure 16. Noise occupancy measurement of the three AFEs implemented in the RD53A chip as a function of the threshold (a) and the PA bias current (b). The SYNC AFE is shown in blue, the LIN AFE in green and the DIFF AFE in violet. The CMS requirement for the maximum noise occupancy is indicated in red. The number of masked noisy pixels is given for each AFE.

noisy pixels disabled. As expected, the average noise occupancy decreases with increasing threshold, regardless of the front-end design. The DIFF front-end shows very good noise performance, with the average noise occupancy several orders of magnitude below the requirement, even for low thresholds. No hits were found in this front-end in 10^6 triggers at higher thresholds, hence a higher number of triggers was sent to evaluate the average noise occupancy. The other two AFEs satisfy the noise requirement down to a threshold of $1000\,\mathrm{e^-}$, which is consistent with the requirement on the detection threshold. Nonetheless, it can be noticed that the fraction of masked pixels is higher in the SYNC AFE.
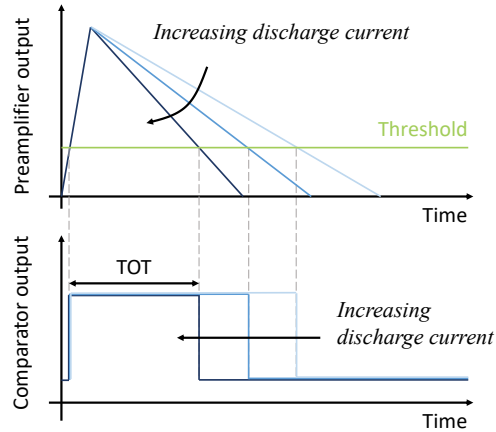
The influence of the PA bias current on the noise was also studied. When this current increases, the transconductance of the input transistor is increased, which results in lower noise with a penalty of an increase in the analogue current consumption. The average noise occupancy was measured for different PA bias currents and is presented in figure 16(b) as a function of the measured analogue current consumption per pixel. All the other front-end settings that could contribute to the current consumption were kept constant during this measurement. As expected the noise in all three AFEs decreases when more current is provided. The DIFF AFE shows again a very good noise performance, with the average noise occupancy well below the requirement, even when operated with low PA bias. The LIN and the SYNC AFE need $3.5\,\mu\mathrm{A}$ and $4.5\,\mu\mathrm{A}$ per pixel, respectively, to reach the required noise level. All three AFEs can meet the CMS noise requirement if the PA bias current is adjusted, hence this parameter is a handle to reduce the front-end noise at the price of an increase in the power consumption.

6 Dead time and time-over-threshold calibration

An important consideration for a highly efficient particle detector is the event loss due to the dead time, especially at high luminosity and high pileup. As explained in section 3 the dead time caused

by the AFE depends on the TOT calibration, and a charge resolution of 3000 e^-/TOT$_{40}$ is necessary to achieve the 1% dead time required for the innermost layer of the IT barrel. The TOT response can be set by adjusting the discharge current of the PA. When the PA discharge current increases, the PA output returns faster to the baseline and the corresponding TOT is smaller, as illustrated in figure 17. Therefore, a faster PA discharge leads to a reduced detector dead time. In the following the required charge resolution of 3000 e^-/TOT$_{40}$ is also referred to as the *fast discharge*.


Figure 17. Sketch of the influence of the discharge current on the signal shape at the output of the PA and on the corresponding TOT.

The TOT charge resolution of the three AFEs was measured with a constant charge injection of 6000 e^- for different PA discharge currents. First, the charge resolution of all three AFEs was set to about 1100 e^-/TOT$_{40}$, as can be observed in figure 18(a). This resolution is not reached for the same current in different AFEs. In the next step, the PA discharge current was increased to verify the front-end compliance with the dead time requirement. As expected, when the discharge current increases the PA discharges faster and the charge resolution is coarser. All three AFEs can reach the required charge resolution indicated by the red line. The SYNC and LIN AFEs can also discharge faster, while the DIFF AFE shows a saturation of the PA discharge current DAC and would be operated at its limit to reach the dead time required for the inner layers.

A dedicated measurement was carried out on the DIFF AFE, to better understand the observed saturation effect. The charge resolution of the DIFF AFE versus the discharge current was measured for different input charges, ranging from 3 to 20 ke$^-$. The result, presented in figure 18(b), confirms the saturation of the discharge current DAC in this AFE, occurring at 30% of the DAC range, regardless of the input charge. This implies a marginal operation of this particular AFE to reach the dead time requirement.

Increasing the discharge current reduces the dead time, as mentioned above, but it also reduces the AFE stability, and therefore it is likely to induce more noise. Hence the noise was re-evaluated for the fast discharge operation. The noise was measured for two detection thresholds, 1000 e^- and 1200 e^-, and two charge resolutions, 1100 e^-/TOT$_{40}$ and the required 3000 e^-/TOT$_{40}$. The combination of these four parameters defined four measurement scenarios for which the average noise occupancy was measured. The measurement method was the same as in section 5. Pixels
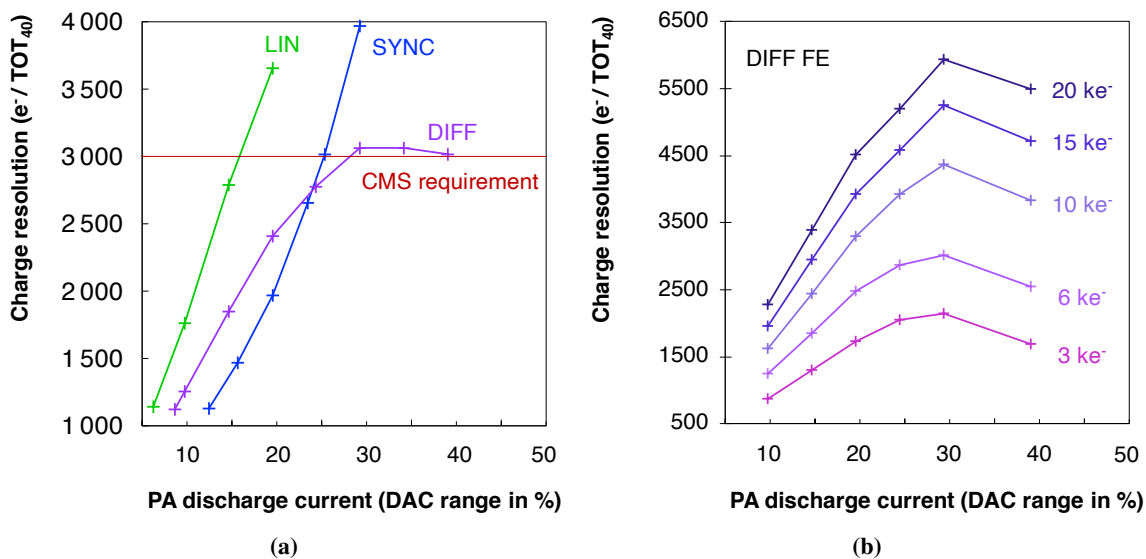
Figure 18. The charge resolution as a function of the PA discharge current (a) measured with a constant charge injection of 6000 e$^-$ for the three RD53A AFEs and (b) measured for different input charges for the DIFF AFE only.

with more than 100 hits in 10^6 triggers were declared noisy and masked, then the average noise occupancy of non-masked pixels was defined as the number of noise hits per pixel and per trigger, measured over 10^6 events.

The fraction of masked pixels is shown in figure 19(a) and the average noise occupancy in figure 19(b) for the four considered scenarios. The average noise occupancy of all three AFEs is higher at fast discharge and is the highest at fast discharge and low threshold, as expected. The DIFF AFE demonstrates again excellent noise performance, with almost no noisy pixels and the average noise occupancy well below the requirement, even at fast discharge. At slow discharge the noise in this AFE was so low that only an upper limit was estimated. The LIN AFE has few noisy pixels and the average noise occupancy satisfies the requirement for any scenario. The SYNC AFE appears to be the noisiest of the three, reaching almost 3.8% of noisy pixels when operated at fast discharge and low threshold. The higher noise in this AFE, significantly increasing with more aggressive chip settings, was considered a critical aspect for the operation in the innermost layer of the CMS Inner Tracker.

7 Late-detected hits

The time response of the pixel readout chip is important to assign detected hits to their corresponding LHC bunch crossings (BXs) and to limit the number of spurious hits from out-of-time pileup interactions. The time response of the AFE, i.e. the combination of the PA rise time and the discriminator speed, is a function of the input charge. Pulses with the same peaking time but different amplitude pass the discriminator threshold at different times. High amplitude signals, depicted in light blue in figure 20, pass the threshold within one BX, i.e. within 25 ns. If the deposited charge is just above the threshold instead, the signal rises more slowly and is detected later by the discriminator.
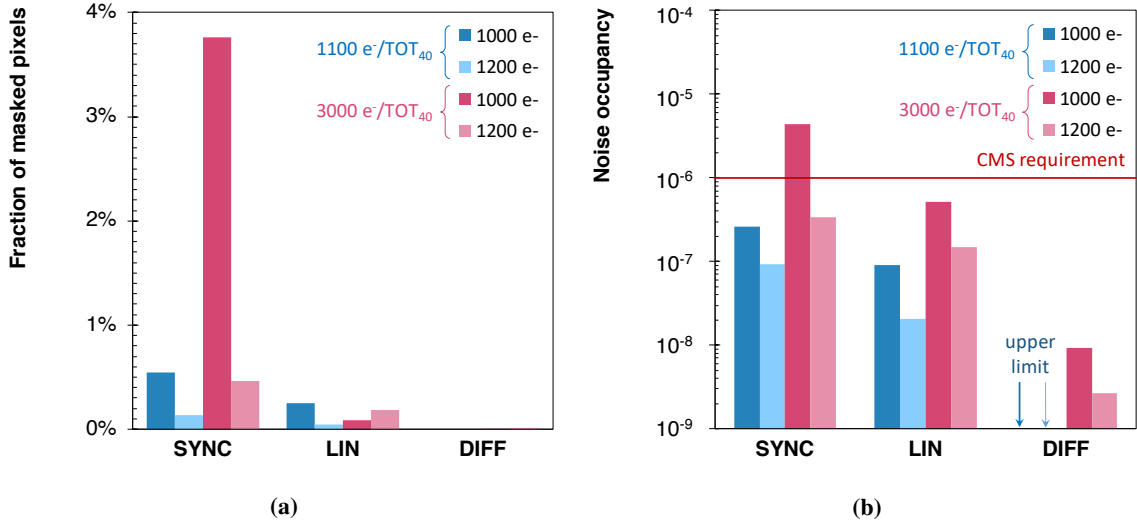
Figure 19. Fraction of masked noisy pixels (a) and the average noise occupancy after masking (b) of the three AFEs in the RD53A chip. The blue colours represent the charge calibration of 1100 e^-/TOT$_{40}$ and the red colours represent the charge calibration of 3000 e^-/TOT$_{40}$. The darker colours are used for the threshold of 1000 e^- and the lighter colours are used for the threshold of 1200 e^-.
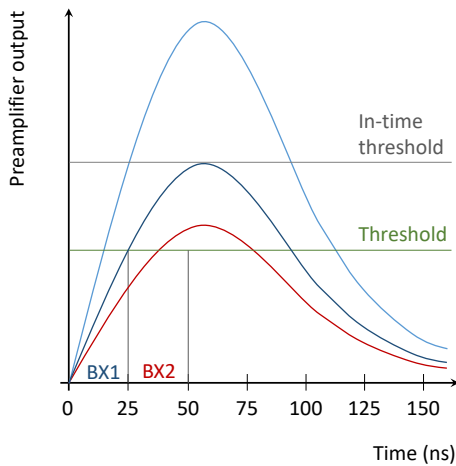

Figure 20. Illustration of the discriminator time response for different signal amplitudes.
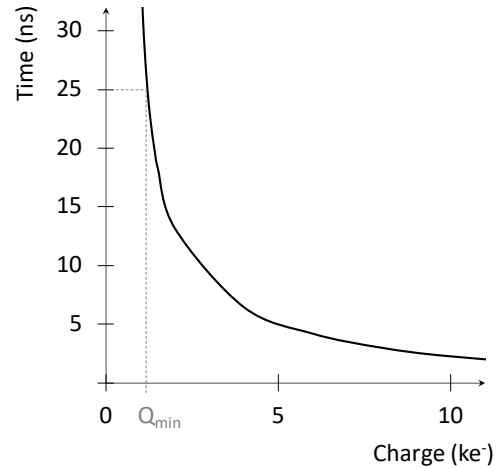
Figure 21. Simulated time walk curve of the linear front-end in the RD53A chip.

Such a hit, shown in red, might be assigned to the following BX, and appears as a spurious hit in another event. The smallest charge (Q_{min}) that can be detected within the correct BX (dark blue signal) is equivalent to the so-called "in-time threshold", which is higher than the threshold of the discriminator. The time behaviour of an AFE is typically described by its time walk curve, i.e. the response delay of the discriminator as a function of the input charge. An example of a simulated time walk curve of the LIN AFE is shown in figure 21. Given that the discriminator of the SYNC AFE is locked to the clock, the following method is used to compare the timing of the three AFEs.

Front-end time response measurement. The charge injection in the RD53A chip can be delayed with respect to the rising edge of the clock with a step size of 1.5625 ns [13]. The front-end time response was measured by injecting calibration pulses with different amplitudes and with different time delays. The detection threshold was set to 1000 e$^-$ and the full range of available charges up to 35 ke$^-$ was scanned, using a finer charge step for low charges where timing is critical. For every pixel the charge was injected 50 times for each time delay. Figure 22 shows the two-dimensional plot of charge versus time for all three AFEs. The x axis represents time in nanoseconds and $t = 0$ indicates the time when the highest charge is detected. The y axis, showing the injected charge in electrons, is limited to 10 ke$^-$ in this figure. The colour code indicates the detection probability for a given BX, for each combination of charge and injection delay. The yellow zone corresponds to 100% detection efficiency, while in the white-coloured region no hit is detected. The left edge of the coloured region corresponds to the time walk curve. In the upper part of the plot, the coloured region is a straight rectangle with a time width of 25 ns, which confirms that high charges are always detected within one BX. Small charges instead are detected later, resulting in a tail in the detection region. This tail extends up to about 40 ns in the SYNC and DIFF AFE, indicating that these two AFEs have a comparable time response. The DIFF AFE is able to correctly assign slightly smaller charges than the SYNC AFE. The LIN AFE appears to be the slowest of the three, with the largest time walk of more than two BXs.
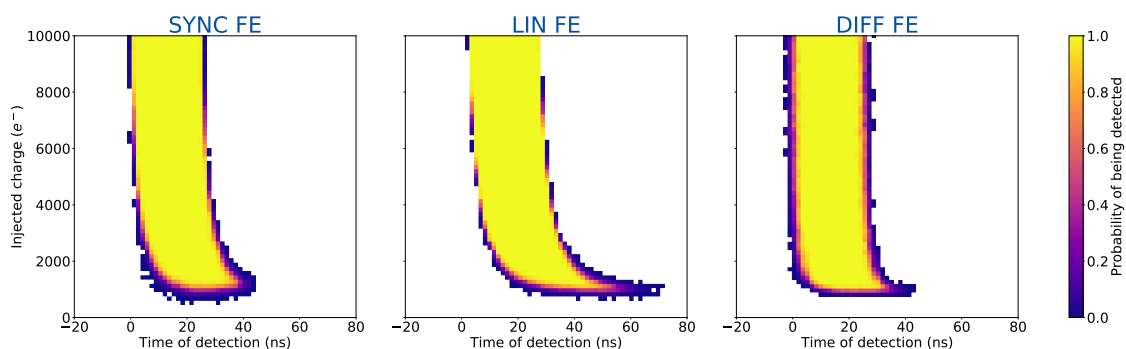
Figure 22. The measured time response of the SYNC AFE (left), the LIN AFE (middle), and the DIFF AFE (right) obtained with one RD53A chip.

Combination with time of arrival simulation. A Monte Carlo simulation was performed within the standard CMS simulation and reconstruction software framework called CMSSW [30] to evaluate the influence of the time response of each AFE on the detector performance and to estimate the resulting fraction of spurious hits. The time of arrival of particles was simulated for different locations in the IT detector, given that it depends on the position of the pixel module with respect to the interaction point. Sixteen different locations were studied: the centre ($z = 0$) and edge module of each barrel layer, the innermost and outermost module of the first and last small disc, as well as of the first and last large disc (figure 1). For each location about 2000 minimum bias QCD events, without pileup and without a transverse momentum cut, were simulated. For the simulation of the beam spot a Gaussian distribution with a width (σ) in z of 4 cm, corresponding to a Gaussian width of 130 ps in time, was simulated. The simulated pixel hits, corresponding to single pixels with

(a) Time of arrival simulation.

(b) AFE acceptance region for a given BX.

(c) Overlay between measurement and simulation.

(d) Late-detected hits.
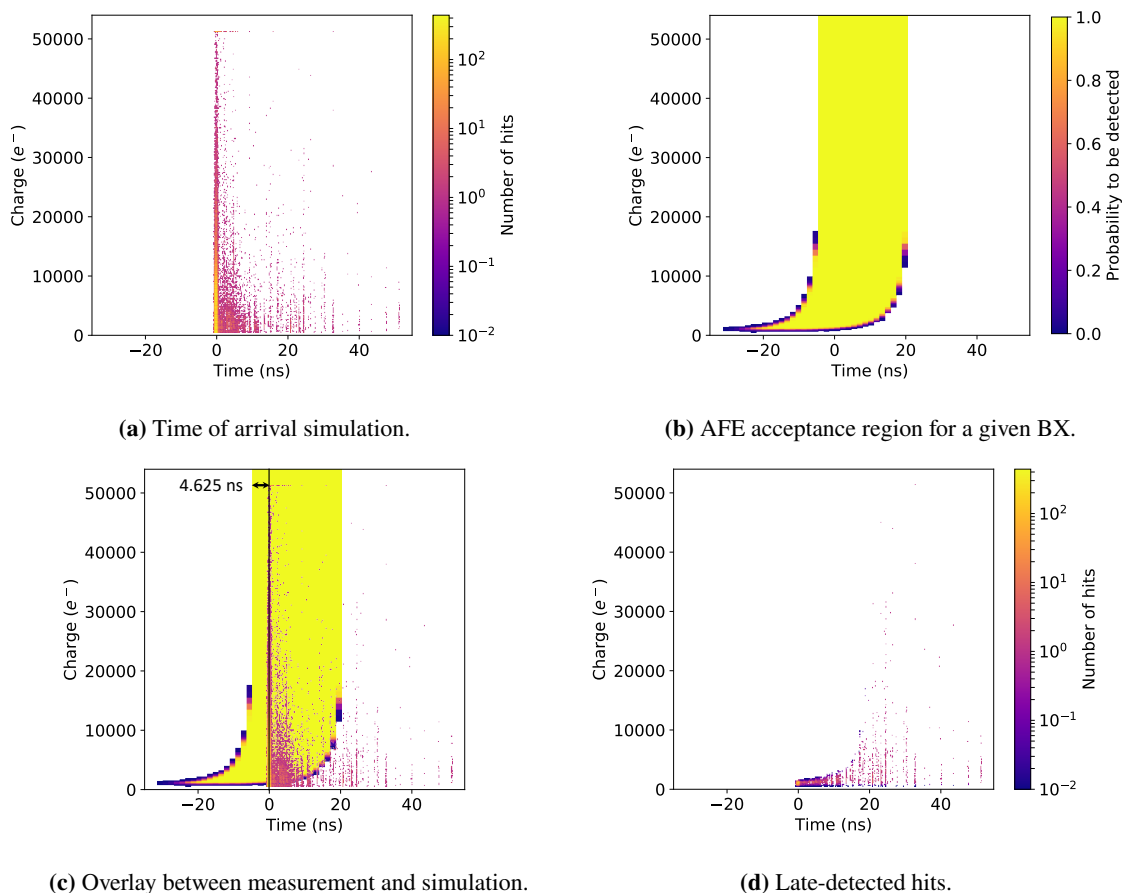
Figure 23. Different steps of the time response evaluation method.

deposited charge, were sorted by released charge, ranging from $600\,\mathrm{e}^{-}$[3] to $50\,\mathrm{ke}^{-}$, with a granularity of $150\,\mathrm{e}^{-}$ and a time resolution of $0.25\,\mathrm{ns}$. The simulated time of arrival versus charge distribution for the central module ($z = 0$) of the innermost layer of the IT barrel is presented in figure 23(a).

Such a distribution was combined with the time response measurement introduced in the previous section. The x axis of the time response is reversed, obtaining the acceptance region, in time and charge, giving the probability of a charge to be detected in the correct BX. This way, instead of showing when a hit is detected by the electronics, the figure indicates when a hit has to occur to be detected in a given BX. The y axis has to be extended to match the charge range in the simulation. Assuming that the time response remains constant for very large signals, the yellow region with sharp edges is extended up to $50\,\mathrm{ke}^{-}$. For illustration, the time response of the LIN AFE, after such modifications, is presented in figure 23(b).

When the acceptance region of the front-end is superimposed with the hit distribution from simulation, as indicated in figure 23(c), the hits that are inside the yellow part of the acceptance region have a 100% probability to be assigned to the correct BX. On the other hand, hits that are outside of the detection region have zero probability to be detected in time. Figure 23(d) shows the

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[3]Given that charges smaller than $600\,\mathrm{e}^{-}$ are not expected to be detected because of the threshold, the simulation started at this charge to avoid overloading the computing time.

hits that will be assigned to a wrong BX, obtained from the exclusion of the two overlaid plots. The integral of the exclusion plot divided by the total number of hits gives the fraction of late-detected hits in a given location of the future detector.

An important part of this method is the time alignment of the two overlapping plots. The origin of the time axis of both the measurement and the simulation have to be correctly aligned. The $t = 0$ of the simulation corresponds to the time when the two proton bunches overlap in the interaction region, corrected with the expected time-of-flight from the interaction point to the given module. The zero of the chip acceptance can be shifted to maximize the overlap, as it would be done in the detector by calibration. For this measurement, the peak of the simulation is placed three fully efficient bins from the left edge of the acceptance region, i.e. 4.625 ns, as it is indicated in figure 23(c). This estimate of about 5 ns was used to account for the imperfect time alignment in the detector due to the variations in the length of the electrical links, jitter, and other contributions, and also including some margin.

Fraction of late hits.   The method described above was used to evaluate the fraction of hits detected late by the three AFE designs. The result is shown in figure 24 for the selected detector locations. The left half of the histogram corresponds to the IT barrel layers, numbered from the centre outwards L1 to L4. For each layer the study was done for two pixel modules, one at the edge (e) and the one in the centre (c) of the barrel. The fraction of late hits increases with the distance from the interaction point. The right half of the histogram is dedicated to the discs, numbered D1 to D12 with increasing distance from the interaction point. For each disc one module on the innermost (i) and one on the outermost (o) ring is presented. For any given disc the fraction of late detected hits is higher on the outer ring.

An ideal front-end with infinitely fast time response was also simulated and the fraction of hits detected late was estimated using the same method described above. Results are shown in grey in figure 24 overlaid to the estimates of the actual analogue front-ends, because they represent the irreducible background. For the considered positions, this fraction is between 0.38% and 7.26%. These are hits generated by particles whose travel time up to the sensor is more than 25 ns longer than the minimum, for which the detector is tuned. The SYNC and DIFF AFE have similar performance, causing few percent of misassigned hits on top of the background. The DIFF is slightly faster. The LIN AFE instead is significantly slower, causing up to additional 11% of late hits in the detector, on top of the irreducible 7% in the worst case.

LIN AFE slow time response mitigation.   Following the outcome of the previous measurement, a modification of the discriminator circuit was proposed by the design team to improve the time response of the LIN AFE. The discriminator is composed of two stages: a transconductance stage and a transimpedance amplifier (TIA). In the TIA two diode-connected transistors, initially introduced to minimise the static current consumption at the output of the discriminator, were forcing other transistors to operate in the deep sub-threshold regime, consequently making them slower. A significant improvement in time walk at the cost of a marginal increase in static current consumption was achieved by removing those two transistors. This led to a simpler TIA stage in the new design of the LIN AFE [31], for the next version of the chip, called RD53B [18].

Circuit simulations were used to extract the time walk curves of both the original and the improved LIN AFE designs. They were transformed into time response plots and combined with
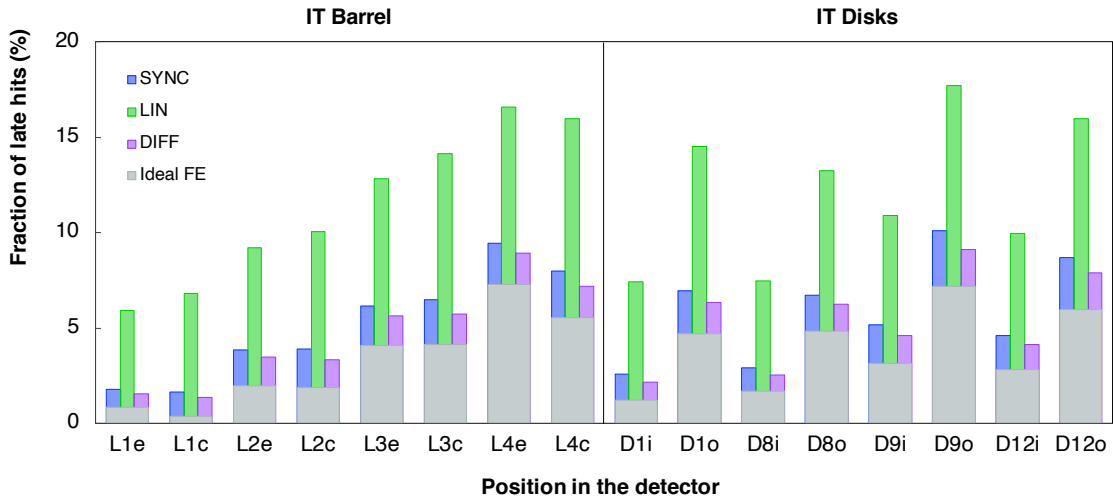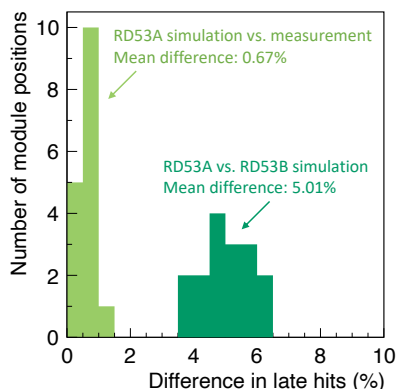
Figure 24. Fraction of hits detected late by the three RD53A AFEs for 16 pixel module positions. The IT barrel layers are numbered from the centre outwards L1 to L4 and for each layer the module at the edge is denoted "e" and the one in the centre is denoted "c". The IT discs are numbered D1 to D12 with increasing distance from the interaction point and for each disc the innermost ring is denoted "i" and the outermost one is denoted "o".

the time of arrival simulations to estimate the fraction of late hits for the simulated designs. The simulated RD53A design was compared to the measurement and the difference in late hits is shown in figure 25. The simulated AFE gives a slightly higher number of late hits. Nevertheless, the simulation demonstrates a very good agreement with the measurement, the difference in late hits being below 1%. This confirms the validity of the simulation, which can therefore be used to predict the fraction of late hits in the improved design. The difference in late hits between the original design (RD53A) and the new one (RD53B) is also shown in figure 25. The new LIN AFE demonstrates on average 5% less misassigned hits. The improved design of the LIN AFE was also implemented in a test chip and verified before and after irradiation. The simulation and measurement results after an irradiation up to 1 Grad confirmed the improvement in time walk, which remains below 20 ns, whereas it increases to around 30 ns in the RD53A version [31].

Late-hit occupancy. The fraction of late-detected hits was converted to the occupancy due to late hits, using the simulated hit occupancies extracted from figure 10. The result is shown in figure 26 for all the positions in the detector. The irreducible background of misassigned hits is almost uniform in the tracker and amounts to between 10^{-5} and 10^{-4}, regardless of the AFE design. The late-hit occupancy levels are at least one order of magnitude above the required noise level, indicated by the red line in the figure. Hence the spurious hit rate in the detector is dominated by the time response of the AFE, not by the noise. Moreover, the performance of the improved design of the LIN AFE is comparable to the other two AFEs, although it remains slightly higher.

Figure 25. Difference between the fraction of hits detected late by the simulated and measured RD53A design of the LIN AFE (light green) and difference between the fraction of hits detected late by the simulated RD53A version of the LIN AFE and the improved RD53B version (dark green).
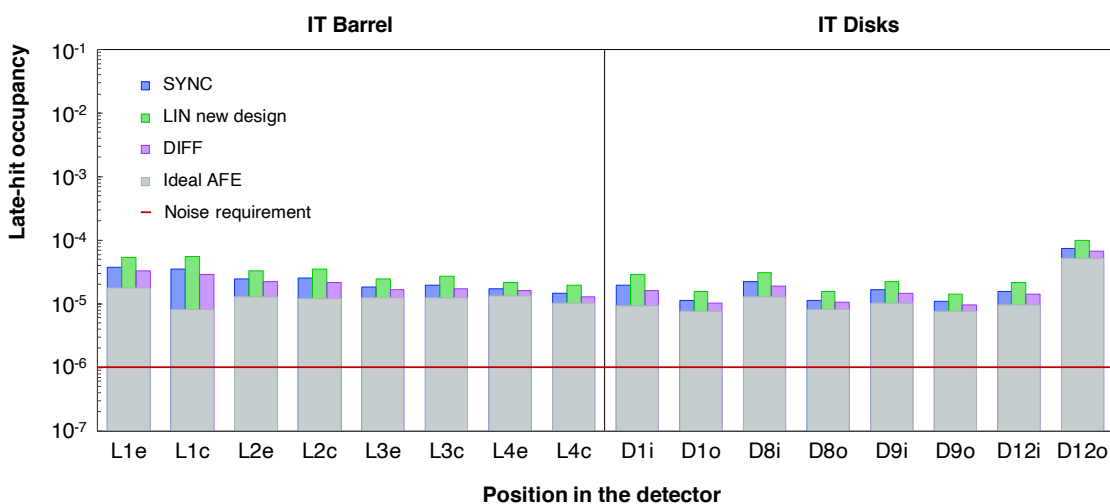
Figure 26. The occupancy due to hits detected late by the RD53A AFEs for different module positions in the detector. The IT barrel layers are numbered from the centre outwards L1 to L4 and for each layer the module at the edge is denoted "e" and the one in the centre is denoted "c". The IT discs are numbered D1 to D12 with increasing distance from the interaction point and for each disc the innermost ring is denoted "i" and the outermost one is denoted "o".

8   Conclusions

A new generation pixel readout chip is being designed for the upgrade of the CMS Inner Tracker to cope with stringent requirements imposed by unprecedented radiation levels and hit rates. Three different analogue front-ends were designed by the RD53 Collaboration and implemented in a large scale demonstrator chip (RD53A). The three designs were characterized and the expected detector performance was evaluated against the requirements to choose the most suitable option for CMS.

The differential analogue front-end showed the best noise performance, with the noise occupancy several orders of magnitude below the requirement, as well as a very good time response. Nevertheless,

this analogue front-end showed a problematic threshold tuning after irradiation, at cold temperature ($-10\,°C$) and with high leakage current. An improved design was proposed, expected to extend the operation with effective threshold tuning up to 500 Mrad, according to the simulation results. A saturation in the preamplifier feedback requires operation at the limits of the time-over-threshold response in order to match the dead time requirement for the innermost layer of the Inner Tracker.

The synchronous analogue front-end features an automatic threshold tuning performed periodically by the auto-zeroing circuit and offers a very good timing performance. However, it appeared to be the noisiest of the three analogue front-ends. The noise increased for lower thresholds and fast preamplifier return to baseline, becoming critical for the operation settings of Layer 1.

The linear analogue front-end satisfied all the requirements, but featured a slower time response. However, an improved design was developed and is expected from simulation to reach a timing performance almost equivalent to the other two analogue front-ends. Since all the performance parameters of this analogue front-end satisfy CMS requirements and the main drawback was addressed and mitigated, the linear analogue front-end was identified as the lowest-risk option for the future pixel detector. CMS selected the linear analogue front-end with an improved design for the integration into the next version of the RD53 pixel chip for CMS (the C-ROC). A prototype is expected to become available in 2021.

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