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A compact CMOS compatible micro-Pirani vacuum sensor with wide operating range and low power consumption

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Abstract

A micro-Pirani vacuum sensor with an operating pressure range of more than 5 decades is described. The device is fabricated by applying a low-resolution and potentially low-cost front-side bulk micromachining step to a chip produced with a commercial CMOS technology. Maximization of the thermally coupled surfaces has been obtained by stacking all layers available by default in the CMOS process. This design choice and the integration of a low-noise, low-power readout interface allowed achievement of state-of-art performances with a fabrication approach affordable even to SMEs and small University laboratories.

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Keywords: Vacuum gauge; CMOS sensors; Micromachining; Thermal sensor; MEMS

1. Introduction

Pirani vacuum gauges, based on air gap thermal conductance dependence on pressure, are particularly suitable to be extremely miniaturized by means of micromachining technologies and many devices with dimensions in the micrometer and nanometer range have been proposed [1]. Research efforts have been devoted to fabricate devices with smaller size, lower power consumption, faster response times and greater operating pressure range. A few devices have matured from the research stage to commercial vacuum gauges [2]. Miniaturized Pirani offers also the possibility of performing in-situ vacuum monitoring inside sealed MEMS packages of inertial sensors, like gyroscopes and accelerometers, optical devices and resonators. Nevertheless, high performances devices have been

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usually fabricated with dedicated technologies [3], different from the standard microelectronic processes used for integrated circuits. This prevents the integration of readout circuits on the same substrate of the sensor and a very few examples of micro-Pirani with on-chip read-out circuits have been proposed [4-6].

In this work, we describe a device that relies on a commercial microelectronic process for most part of the fabrication flow. The sensing structure consists of a heater and a temperature probe placed on two different cantilever beams separated by a small air gap. The novelty with respect to previous designs is the stacking of all layers available by default in the CMOS process on the cantilever tip in order to maximize the heat exchange. Furthermore, an electronic interface based on a low-noise, low-power instrumentation amplifier is integrated on the same chip. In this way, a device operating over a more than 5 decades pressure range has been obtained.

2. Device description

The layout and cross section of the proposed sensing structure are schematically shown in Fig. 1. The two opposite cantilevers, suspended over a cavity, are separated by a 5 μm air-gap. One cantilever supports a polysilicon heater (1.5 kΩ), while a 10-element *n*-polysilicon/*p*-polysilicon thermopile is placed on the other one. The thermopile detects the temperature difference between the cantilever tip and the substrate, which, for a fixed heater power, is roughly proportional to the pressure dependent air-gap thermal conductance [5]. This property has been also used for the compensation of the pressure effects on the response of gas flow sensors based on a heat transfer principle [7,8]. In order to increase the air-gap cross-section, the thick upper aluminum interconnect layer (3 μm thick) has been placed on the tips of both cantilevers. In this way, we increase the thermal conductance between the two cantilevers with positive effects on the device sensitivity.

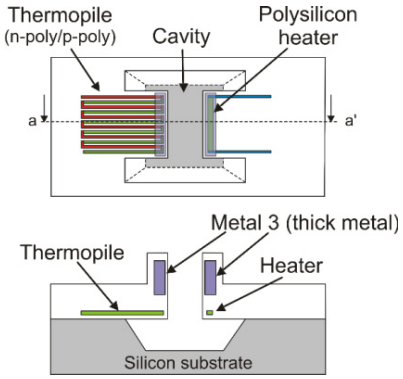

Fig. 1: Schematic top view and cross-section of the proposed micro-Pirani (not to scale).

The chip has been designed using the BCD6s process of STMicroelectronics and the portion with the sensing structures and the read-out circuit is shown in the optical micrograph reported in Fig. 2. Two identical sensing structures have been integrated in order to verify the repeatability of the fabrication process. The electronic interface includes a low noise (19 nV/√Hz), low offset (< 2 μV) chopper amplifier with gain=200 and a low noise programmable current source to read the thermopile voltage and bias the heater, respectively. The cavity underneath the cantilever has been obtained by applying a simple post-processing sequence to the chip returned from the silicon foundry. Details about the post-processing steps are reported in [9]. Briefly, openings into dielectric layers have been defined in the front side of chip with a RIE (reactive ion etching) in CF_4/Ar (50%/50%) gas mixture using an 8 μm thick photoresist film (MEGAPOSIT™ SPR™ 220–7.0) as a mask. Then, the silicon substrate has been anisotropically etched for 150 min at 85 °C in a solution of 100 g of 5 wt% TMAH with 2.5 g of silicic acid and 0.7 g of ammonium persulfate. Due to the fast degradation of the TMAH solution [10], the silicon etching has been performed in three separate 50 min long steps, each one performed with fresh reagents. The magnification of the two identical sensing structures after the silicon removal is reported in Fig.2. After the post-processing, the chip was glued to ceramic DIL 28 packages using wedge bonding to connect pins to pads.

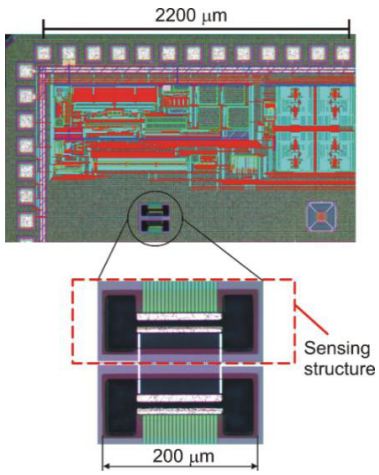

Fig.2. Optical photograph of the test chip portion including the sensing structure and the readout interface. The magnification shows two identical sensing structures after the silicon etching. The layout of the readout interface is superimposed on the photograph to show the electronic circuits buried below the planarization dummies.

3. Experimental results

The devices have been characterized in a vacuum chamber pumped down by a mechanical pump and a turbo pump. For the measurements, the chamber has been pumped down to a residual pressure of 10^{-3} Pa and then it has been separated from the pumps by a vacuum valve and slowly vented with air to atmospheric pressure. The dependence of the output voltage on pressure for a heater current of 0.88 mA is shown in Fig. 3. The total power consumption, including the interface, is 3.56 mW. Note that the raw data (open circles) tend to settle to nearly 3 mV at the lowest pressures. This residual voltage has been found to be proportional to the heater power and has been then ascribed to parasitic thermal conduction paths occurring through the substrate. Subtracting the residual voltage extended the pressure range down to 0.3 Pa, as shown in Fig. 3.

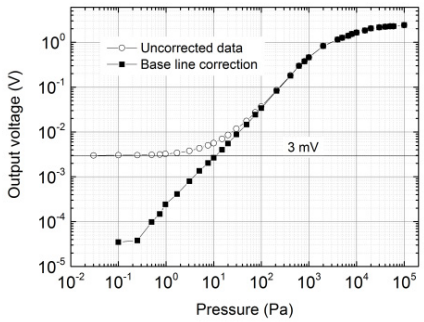

Figure 3: Output thermopile voltage (amplified by 200) as a function of pressure for a 0.88 mA heater current. Corrected data (filled squares) have been obtained from raw data (open circles) by subtracting the 3 mV residual voltage.

The sensor sensitivity and resolution of the device have been calculated and shown in Fig. 4. The sensitivity has been calculated differentiating the corrected response curve of Fig. 3 while the resolution has been obtained as the peak-to-peak output noise (100 μV) over sensitivity ratio. It can be seen that the resolution gets worse at high pressure due to the sensitivity drop but it remains better than 100 Pa up to atmospheric pressure. So a relative accuracy better than 0.1 % of full scale is maintained up to atmospheric pressure, allowing operation over a more than 5 decades pressure range.

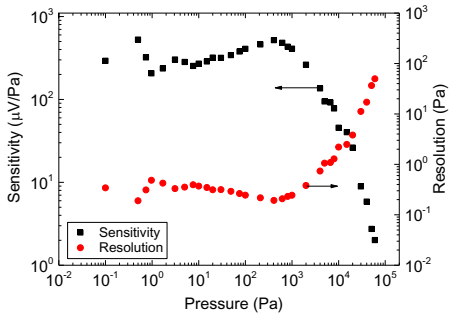

Figure 4: Sensor sensitivity (derivative of the corrected response curve of Fig.3) and resolution as a function of pressure.

Sensitivity of devices based on heat transfer is proportional to power [9] so device performances could be improve increasing the current fed to the heater on condition that the maximum operating temperature has not been reached. In order to verify this possibility, the heater resistance and overheating, estimated from the temperature coefficient of resistance, have been measured as a function of pressure and the result is shown in Fig. 5. It can be seen that the overheating is less than 38 °C suggesting that there is wide margin to reliably increase the heater current in order to improve the sensitivity.

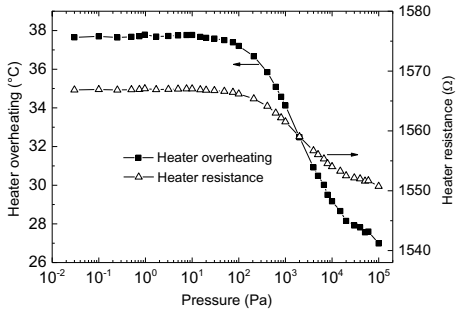

Figure 5: Heater resistance and overheating as a function of pressure. Overheating has been calculated from the resistance using the temperature coefficient of the heater material (*p*-polysilicon) resistivity, reported in the process design manual.

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