The New Readout System of the NA62 LKr Calorimeter

A. Ceccucci, R. Fantechi, P. Farthouat, G. Lamanna, J. Rouet, V. Ryjov, and S. Venditti

***Abstract*—The NA62 experiment [1] at CERN SPS (Super Proton Synchrotron) accelerator aims at studying Kaon decays with high precision. The high resolution Liquid Krypton (LKr) calorimeter, built for the NA48 [2] experiment, is a crucial part of the photon-veto system; to cope with the demanding NA62 requirements, its back-end electronics had to be completely renewed. The new readout system is based on the Calorimeter REAdout Module (CREAM) [3], a 6U VME board whose design and production was sub-contracted to CAEN [4], with CERN NA62 group continuously supervising the development and production phase. The first version of the board was delivered by the manufacturer in March 2013 and, as of June 2014, the full board production is ongoing. In addition to describing the CREAM board, all aspects of the new LKr readout system, including its integration within the NA62 TDAQ scheme, will be treated.**

***Index Terms*—Data acquisition, digital signal processors, high-speed electronics.**

I. The NA62 Experiment

THE NA62 experiment at CERN will study several Kaon decays with unprecedented statistics. Its main goal is the measurement of the ultra-rare $K^+ \to \pi^+\nu\bar{\nu}$ decay's branching ratio (BR), whose precise theoretical prediction within the Standard Model (SM) framework [5] has a sub-10% total error but can presently be compared with an experimental measurement based on seven candidate events [6] only. The collection of about 100 events with $\sim 10\%$ background will allow to test the SM in a complementary way to the LHC studies, and to probe the presence of new physics in the Kaon sector.

A view of the NA62 experiment is shown in Fig. 1. Kaons produced by the 400 GeV/c SPS protons impinge on a Beryllium target; outgoing charged particles are selected in a 75 GeV/c $\pm$ 1% momentum band. Before the decay region, Kaons are identified by the Cedar, a gas-filled Cherenkov detector, with 10^{-3} inefficiency, and their momentum and direction measured with high precision by the Gigatracker, made of 3 silicon pixel stations. The CHarged ANTI counter (CHANTI) detector vetoes particles produced by inelastic scattering of beam particles in the last Gigatracker station.

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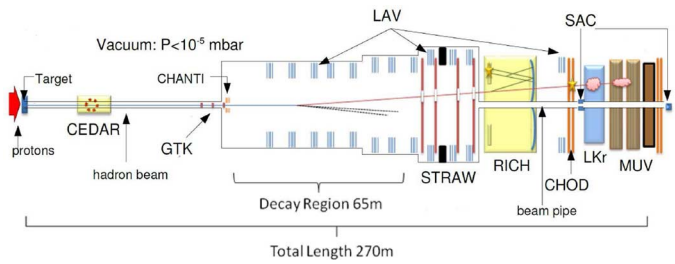

Fig. 1. The NA62 experiment.

The veto system aims at detecting particles from several Kaon decays (especially γ s originating from π^0 s, whose detection inefficiency must be be $< 10^{-8}$ in order to attain the required S/B ratio) that would otherwise represent a background (BG) for the $K^+ \to \pi^+\nu\bar{\nu}$ decay measurement. It is made of 12 Large Angle Veto stations (LAVs) along the beamline, made of lead-glass crystals from the OPAL [7] calorimeter, the Liquid Krypton (LKr) calorimeter, described in more detail in Section II, and two Shashlik-based detectors, the Intermediate Ring (IRC) and Small-Angle (SAC) Calorimeters, used to increase the LKr calorimeter acceptance at low angles and to detect photons decaying along the beamline, respectively.

The Straw system measures the momentum of charged particles from Kaon decays. It is made of four chambers (two before and two after a magnetic field), each made of four views/chamber; each view has four staggered straw layers, for a total of 112 straws/layer. Straws are filled with Argon and CO_2(70/30%); a high spatial precision (130μm/view) and a low mass budget ($\sim$ 1.8%X_0) are key requirements for this detector.

The Ring Imaging CHerenkov (RICH) detector provides Pion identification at $5 \cdot 10^{-3}$ inefficiency by reconstructing the Cherenkov cone produced by charged particles crossing a Helium tank.

The MUon Veto (MUV) system yields pion energy measurement (MUV1 + 2, iron/scintillator sandwich) and muon rejection (MUV3, scintillator tiles).

The largest BG rejection of the $K^+ \to \pi^+\nu\bar{\nu}$ decay ("constrained BG") is obtained by selecting two regions of the $M^2_{miss} = (P_K - P_\pi)^2$ variable distribution, whose computation requires the high-precision measurement of the incoming Kaon and Pion four-momenta by the Gigatracker and by the Straw system, respectively. The rejection of the residual BG ("non-constrained BG") is obtained through particle identification by the RICH and the Cedar and through additional particle detection by the veto system. The distributions of the constrained and non-constrained BG as a function of the M^2_{miss}

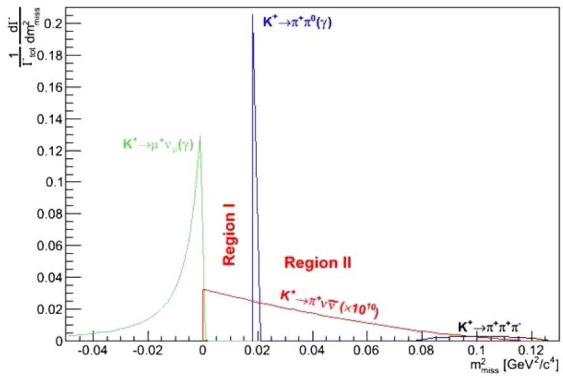

Fig. 2. Constrained BG.

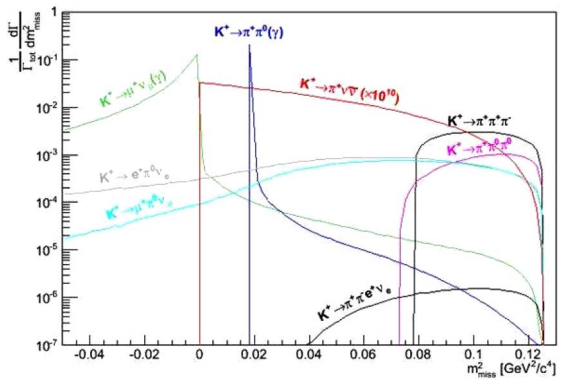

Fig. 3. Non-constrained BG.

variable for the most sizable Kaon decays are shown in Figs. 2 and 3.

Three trigger levels will be implemented to reduce the 10 MHz Kaon decays in the fiducial region down to the 10 kHz events written on disk, each level reducing the data load by about one order of magnitude. The first trigger level (L0 T) is FPGA-based and will use the TEL62 board [8], developed by the NA62 collaboration and based on the TELL1 board [9] from the LHCb experiment, in order to produce the trigger primitives of the detectors participating in the L0 T decision. A central L0 processor will collect all the trigger primitives, take a decision (the detectors involved in the decision depend on the type of trigger) and distribute the L0 T to the readout system of all detectors through the TTC system. The latency of the L0 T decision will be fixed and equal to about 1 ms.

The two higher trigger level decisions will be taken by a PC farm and their latency is not fixed. The second level trigger (L1 T) algorithm will take a L1 T decision using data collected at L0 in $\sim$ 1 s and distribute the L1 T signals to the detectors that didn't send their data to the PC farm before. After this data is collected, the third trigger level algorithm (L2 T) is applied, its latency being as long as the SPS cycle. Events accepted by the L2 T are written on disk. A scheme of the NA62 TDAQ system is shown in Fig. 4.

II. The NA62 Liquid Krypton Calorimeter

NA62 will reuse the quasi-homogeneous LKr calorimeter built for the NA48 experiment (Fig. 5). Its goal is to veto particles from BG decays, as part of the NA62 veto system, and to measure electromagnetic energy deposits with high precision. The calorimeter is made of $\sim$ 10 m^3 liquid Krypton at 120 K, housed inside a cryostat. The LKr volume is divided into 13248 2×2 cm^2 cells by Cu-Be electrodes (Fig. 6), which have a pointing geometry and a zig-zag shape to minimise response inhomogeneities when the particle shower is too close to the anode.

The signal produced by a particle crossing the LKr is collected by preamplifiers mounted inside the cryostat, directly attached to the calorimeter strips, and is then sent out using 50Ω coaxial cables and feedthroughs on the top of the cryostat. The signals are then sent to the transceiver boards, plugged directly on the feedthroughs and sharing the Faraday cage made by the cryostat. The board performs a pole-zero compensation, recreating the $\sim$ 20 ns rise time and $\sim$ 2.7 μs total length triangular signal shape given by the calorimeter cell, previously shaped by the $\tau = 150$ ns decay constant of the preamplifier. The output signal is sent to the readout system through cables housing 16 twisted pairs each. The whole process is summarized in Fig. 7.

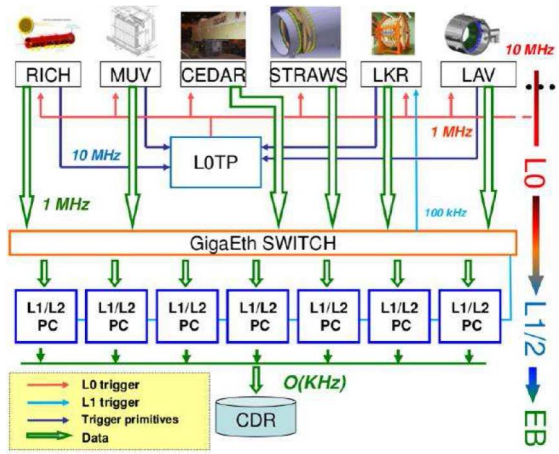

Fig. 4. The NA62 TDAQ system.

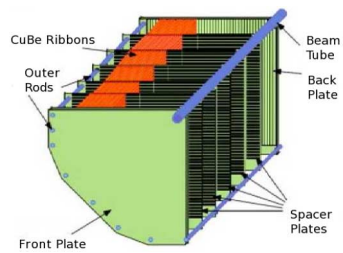

Fig. 5. Calorimeter's layout (one quadrant).

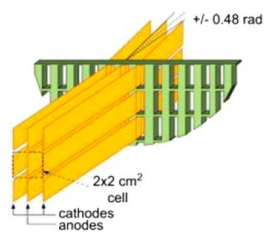

Fig. 6. Detail of the LKr calorimeter's cells.

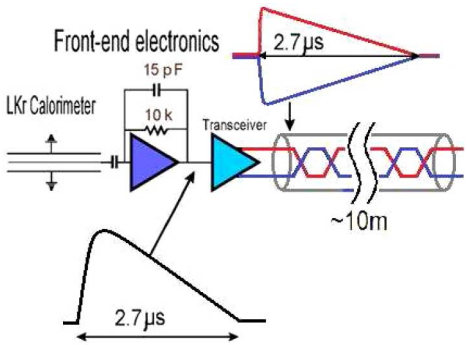

Fig. 7. Analog signal from the detector to the readout system.

Fig. 8. The CREAM module(front view).

To control the response uniformity and stability of the whole calorimeter, a calibration system based on about 2000 pulse generators has been implemented. Each generator produces an exponentially decaying signal that serves 8 channels; its pulse height is set by a 15 bit DAC.

III. The CREAM Module

The CREAM, shown in Fig. 8 and 9, is a 6U VME 64 board developed by CAEN, under specifications provided by the NA62 and the PH-ESE CERN groups. It consists of a daughterboard, where the analog input signals are shaped and digitised, and a motherboard, where the data is processed and eventually sent out if the required trigger conditions are met. A CREAM-based readout system has replaced the old LKr readout system [10], unable to cope with the demanding NA62 requests in terms of rate sustainability and trigger logic.

The CREAM block diagram is shown in Fig. 10. A total of 432 CREAMs are needed to read all LKr cells, requiring 28 VME crates (up to 16 CREAMs/crate are needed, depending on the LKr geometry); a crate can host up to 19 CREAMs housed in 8 racks located above the LKr cryostat.

The CREAM configuration is provided via the VME bus. A PC equipped with a four-channel optical link PCIe card can control up to 8 daisy-chained VME bridges per link, thus handling the configuration of all CREAMs. A set of configuration libraries developed by CAEN are available; the board firmware can be updated through either the VME backplane or JTAG.

Fig. 9. The CREAM module(side view).

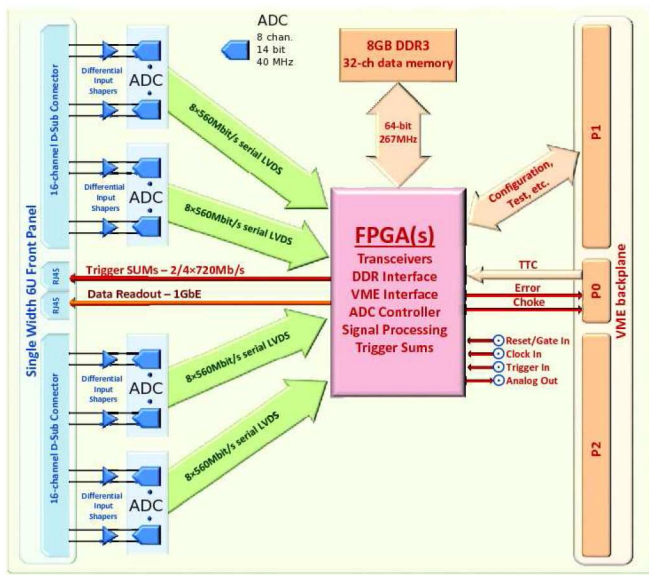

Fig. 10. The CREAM block diagram.

A. The Analog Signal Processing

Signals from the LKr arrive to the CREAM as 16 differential, individually shielded pairs for each 50-pin connector (type 2 ITT-Cannon DD-50P); each CREAM has two such connectors mounted on the daughterboard, for a total of 32 channels. The input signals are AC coupled and have a maximum amplitude of ± 1 V; their shape is triangular, with 20 ns rise-time and 2.7 μs total length.

Before being sent to the ADCs, the signal is shaped by first differentiating it with a 20 ns time constant and then by feeding it into a 9-pole Bessel filter (Fig. 11). The result is a 70 ns FWHM pseudo-gaussian, followed by an undershoot at about 3% of the pulse amplitude which lasts for a time equal to the drift time of the electrons across the calorimeter cell.

B. The Signal Digitisation

After having being shaped, the signals are digitised by the AD9257 chip [11] from Analog Devices, using the 40.08 MHz clock distributed by the TTC-LKr module as sampling clock. The AD9257 chip is a 14-bit, $2V_{pp}$ range, 8-channel serial output ADC; 4 such chips, placed on the daughterboard, are

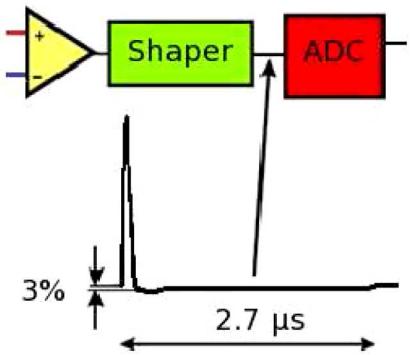

Fig. 11. Analog signal shaping before the ADCs.

required to digitise all the input signals of a CREAM. The baseline of each channel can be set by a 16 bit DAC to fully exploit the available dynamic range (during normal data-taking the baseline of each channel will be set at about 400 ADC counts). Samples from each chip are then serialised and sent to an Altera Stratix IV FPGA mod.EP4SGX180 [12] mounted on the motherboard. Here data is continuosly copied on a circular 256 Mbit buffer implemented in a 8 GB storage capacity DDR3 SODIMM module, waiting for a L0 T signal. The maximum latency allowed by this buffer is 12.5 ms, whereas the typical latency required for the L0 T decision will be of about 1 ms.

C. The Trigger Signal Processing and Output Data

The CREAM data flow is shown in Fig. 12. When the CREAM receives a L0 T signal through the custom backplane, a configurable number of samples (up to 256) is extracted from the circular buffer at fixed, but configurable, latency and copied into the 255×256 Mbit wide L0 buffer, implemented in the DDR3 module, which can contain up to 16 seconds data-taking ($>$ SPS spill duration) at the nominal L0 T rate of 1 MHz and for 8 samples/channel extracted. The event is uniquely identified by an event number and a timestamp (in 25 ns units), associated with each trigger. The trigger type is specified by a 6-bit word received by the CREAM immediately after the L0 T signal through the backplane. The CREAM firmware allows to interpret several types of trigger dispatched by the L0 trigger processor (L0 TP); for each of them a different action is performed.

A L1 T decision is notified by the PC farm to the CREAM through a UDP packet sent to the Data Link(DL), a RJ45 connectors on the front panel featuring a 1 Gbit/s Ethernet I/O link. Each Multi-Request Packet (MRP) can contain up to 100 L1 T requests, each of them specifying the event number of the requested event. CREAM data corresponding to the requested event number is sent as a Sub-Detector Event (SDE) UDP packet to the PC farm through the same link, the IP address of the requesting PC being automatically retrieved from the MRP by the CREAM firmware. Data from the DLs of the 16 CREAMs in the same crate is collected by a switch (Figs. 13 and 14), which routes all the data packets to the PC farm through a 10 Gbit/s optical link. 2

The MRPs are sent to the CREAMs in multicast mode, provided that the CREAMs have previously joined a proper multicast group by issuing a IGMP packet. This feature reduces the

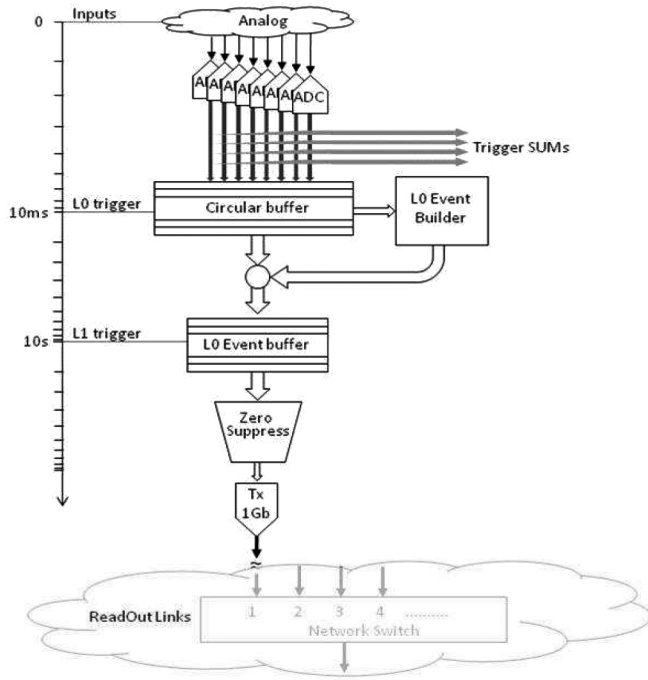

Fig. 12. The CREAM data flow.

Fig. 13. CREAM data links to the switch.

Fig. 14. The switch collecting all data links of a crate.

network traffic (request packets are distributed at switch level to all the CREAMs) and also allows an easy way to define LKr regions of interest: different calorimeter regions can join different multicast groups, thus requiring only a part of the LKr data on the basis of data used for the L1 T decision.

Besides the normal data acquisition mode, in which data from all channels is sent to the PC farm when a L1 request reaches the CREAMs, other acquisition modes can optionally be activated:

- Continuous mode: 65536 samples (corresponding to about 1.6 ms data-taking) per channel are sent to the DL when the acquisition is activated;
- L0 readout mode: Packets are sent to the DL when a L0 signal is received through the custom backplane;
- Zero-suppression mode: the CREAMs send out only data of those channels having at least one sample above a configurable threshold value.

In addition to the lines used to deliver the TTC information to the CREAMs, the custom backplane also hosts 20 CHOKE and 20 ERROR single-ended CMOS lines, one for each CREAM slot. A CHOKE line is driven high to indicate that the CREAM module memory is overloaded with data and approaching a situation in which triggers cannot be served without losing data. The assertion of a CHOKE signal by one CREAM is notified by the TTC-LKr to the L0 T central processor, that stops the L0 T dispatching and distributes a CHOKE ON L0 trigger to all detectors. When the overloading problem is solved, the CHOKE signal is driven low and the L0 T dispatching can restart, the first dispatched L0 trigger being a CHOKE OFF. In a similar way, if, in spite of the choke signal, L0 T signals cannot be served, or if a generic error occurs, an ERROR signal is raised.

D. The Trigger Sum Link (TSL)

The information from CREAMs cannot be fully exploited to take a L0 T decision, because the bandwidth required to move the corresponding data to the L0 T processor would be too large. Even sending all LKr data to the PC farm after a L0 T signal would require about 2 Tbit/s bandwidth.

On the other side, the information from the LKr detector is fundamental to obtain the rejection power required by the NA62 trigger system, especially at the L0 T level. For this reason the sums of the digitised signals from 4×4 cell tiles are computed by the CREAM firmware every 25 ns and sent to the LKr L0 T processor (LKr L0 TP).

The sample value from each channel is first individually baseline-subtracted and gain-adjusted to take into account the differences between channels (mainly due to different preamplification factors and different gains of the ADC channels). The sum is then computed and the result serialized (the two LSBs are neglected, so that only 16 bits are transmitted) and sent out through a RJ45 connector on the front panel, the so-called Trigger Sum Link(TSL). Two such sums are produced by each CREAM and serialized on two individually shielded pairs of an Ethernet cable (the other two pairs are unused). The serialization is done in the FPGA according to the specifications of the DS92LV16 chip datasheet [13].

The serialised data is collected by the TELDES board [14], developed by the NA62 collaboration and mounted on a TEL62. Each TELDES board receives up to 8 TSL cables (each carrying 2 tile sums) from the CREAMs and mounts 16 DS92LV16 chips, each deserializing the digital sum from one 2x8 tile every 25 ns. The deserialised data is then sent to the TEL62 through a 200-pin connector.

The LKr L0 TP, implemented in the TEL62 FPGAs, looks for maxima in energy deposits in space and time and computes the total energy deposit in the calorimeter or in its quadrants. The process takes place in two steps, with maxima being searched first in the horizontal and then in the vertical direction of the LKr surface; the final information (number of energy peaks, their energy and time) is then used for the final L0 T decision. A TEL62 mounting two TELDES boards is shown in Fig. 15.

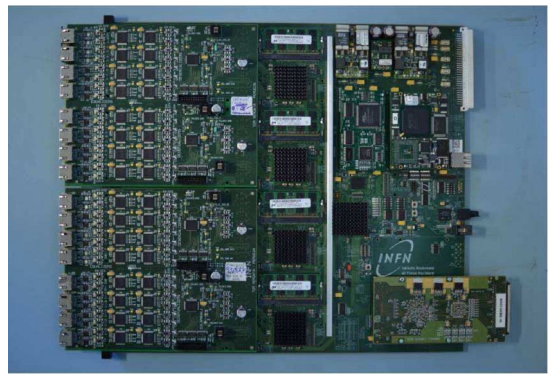

Fig. 15. A TEL62 mounting two TELDES boards.

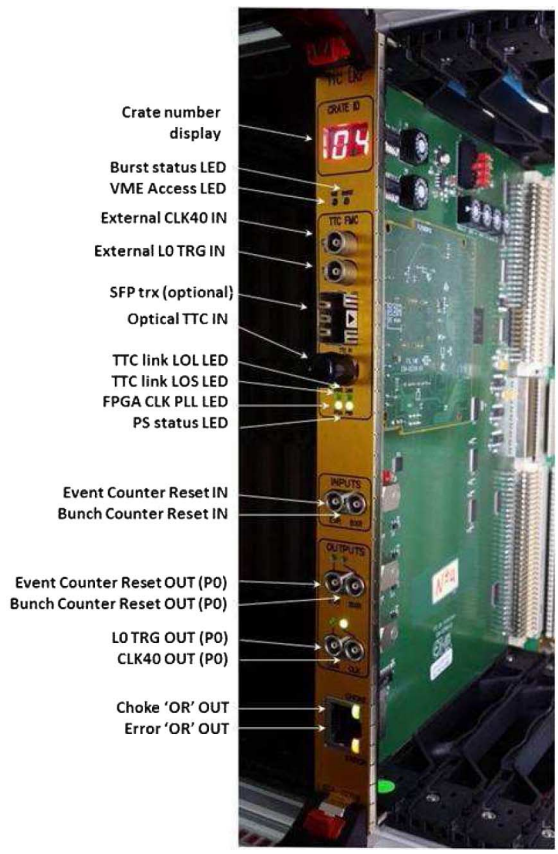

Fig. 16. The TTC-LKr board.

IV. The TTC-LKr Board

The TTC-LKr board [15] (Fig. 16), developed by the CERN PH-ESE group, receives the clock and the L0 T signal information through the optical TTC [16] signal, decodes it and distributes it to all CREAMs in the same crate on a custom backplane. The TTC-LKr is a 6U VME 64x board mounting a Xilinx Spartan-6 FPGA, on which a TTC-FMC mezzanine using the ADN2814 [17] data recovery IC is plugged. The board is placed in the 11th slot of each VME crate.

The TTC is a unidirectional optical fiber based transmission system where two channels, A and B, are multiplexed and encoded using the LHC 40.8 MHz clock and transmitted at 160 MHz rate. One channel is used to carry the L0 T signal only, while the other carries the clock and the information concerning resets, trigger type, calibration and monitoring.

The TTC-LKr board turns the TTC information into M-LVDS signals and distributes them to all CREAMs using a custom

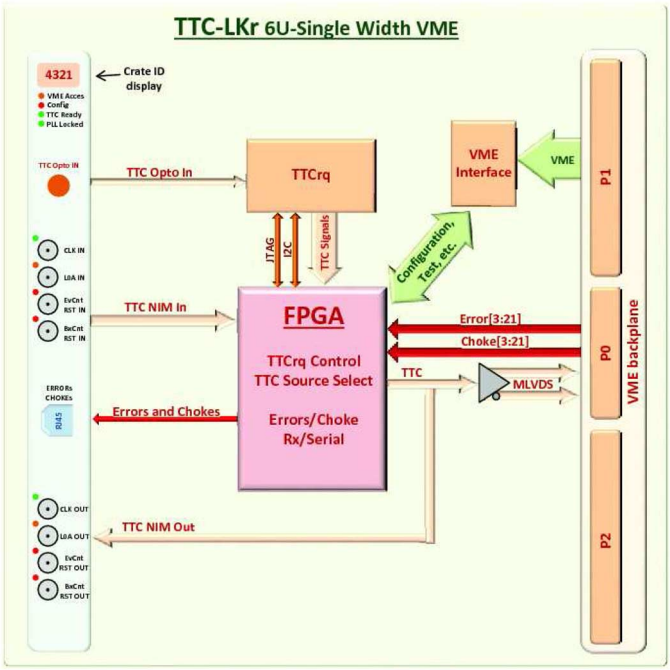

Fig. 17. The TTC-LKr board block diagram.

backplane, which is also used by each of the 16 CREAMs to signal the presence of a CHOKE or ERROR condition. Apart from the optical source, the TTC-LKr board can be configured to provide the clock and L0 T signal through front panel input, the VME bus or an internal generator. The block diagram of its firmware is shown in Fig. 17.

V. Project Status

The development and production of the CREAM board was awarded to CAEN in September 2011. The technical specifications were provided by the NA62 and PH-ESE CERN groups, in compliance with the requirements of the NA62 experiment; the same groups were also actively involved in the supervision and testing of both the hardware and the firmware properties of the board.

In November 2012, during the NA62 test beam, signals from 8 LKr calorimeter cells were digitised by a CREAM daughterboard and collected through a custom readout system, the CREAM motherboard not being available at the time. The signal produced by real particles was thus investigated, this being the only occasion before the the start of the NA62 data-taking period, due to the SPS long shutdown until October 2014.

The first four CREAM prototypes, complete with a preliminary version of the firmware, were delivered to CERN in March 2013. In spring/summer 2013, the analog performances of the CREAM boards were validated during extensive tests at CERN. In particular the following properties were tested:

- Effective number of bits (ENOB) $>$ 10 LSB for a 5 MHz input signal (Fig. 18)
- Integral non-linearity (INL) $<$ 5 LSB (Fig. 19)
- Differential non-linearity (DNL) $<$ 2 LSB (Fig. 19)
- Cross-talk < -70 dB
- 40 ns rise time

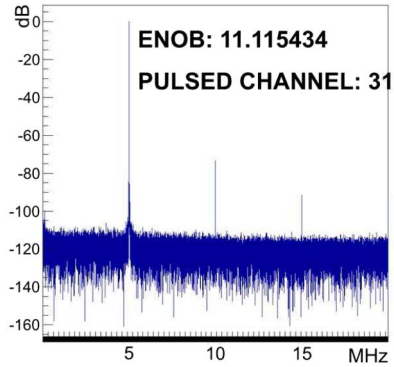

Fig. 18. ENOB estimation.

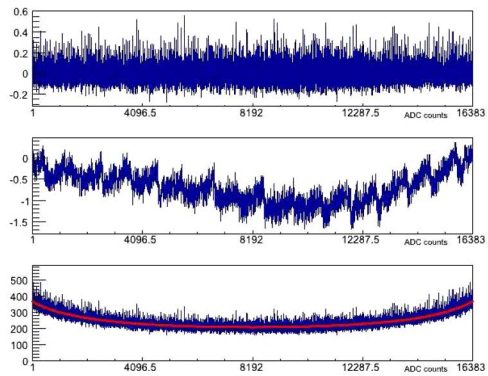

Fig. 19. Integral and differential non-linearities (estimated as in [18]).

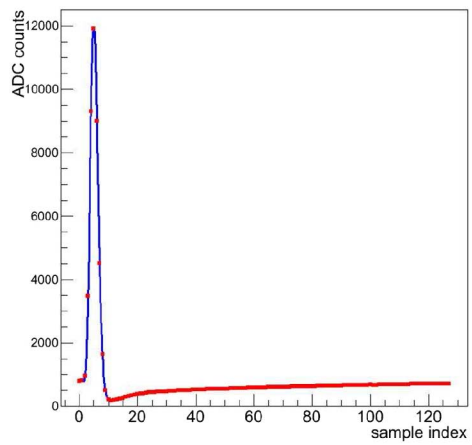

Fig. 20. LKr calibration pulse (128 samples).

- 70 ns $\pm$ 10% FWHM signal width, $\pm$1% uniformity
- Non-coherent noise $<$ 2 LSB, coherent noise $<$ 10% of non-coherent noise

In October 2013 the CREAM pre-production batch, made of 11 boards, was delivered at CERN. These boards allowed to instrument a whole crate during the NA62 test run in November/December 2013, and to test the integration of the CREAM readout with the NA62 acquisition system. Acquisition tests using the LKr calibration system were also performed: in Fig. 20 a calibration pulse is shown, complete with the 2.7 μs long undershoot and collected using the full NA62 acquisition system.

The delivery of the full CREAM production started in March 2014 and is expected to finish in July 2014. To date (June 16th) two thirds of the CREAM boards required to readout the LKr have been installed and their basic functionalities have been tested. The objective is to have a fully operational readout system by October 2014, when the official NA62 data acquisition phase will start.

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