

The TRIMAGE PET Data Acquisition System: initial results

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Abstract—We present the first results obtained with a prototype of the PET read-out electronics of the trimodal PET/MRI/EEG TRIMAGE scanner. The read-out is based on the 64-channel TRIROC ASIC and on an acquisition board that will control up to 12 ASICs. The output of each ASIC is processed in parallel and sent to a host system that in the final version will receive data from 18 acquisition boards. Blocks of 64 SiPMs are one-to-one coupled to a dual-layer staggered LYSO crystal matrix and read by a single ASIC. The FPGA reads the sparse output from the ASICs and reconstructs for each event a full image of the light pattern coming from the LYSO matrix. This pattern can be then processed on-line or sent to the host PC for post-processing. Early tests were conducted by using a prototype board with single LYSO crystals of $3.3 \text{ mm} \times 3.3 \text{ mm} \times 8 \text{ mm}$ and dual layer staggered LYSO matrices. Results show that the ASIC can sustain input rates above 58 kHz on all its channels, with small variations depending on the discriminating thresholds, being this limit due its digital output stage. With the single crystals setup, we obtained an energy resolution of 10.7% at 511 keV and a coincidence time resolution of 420 ps FWHM. With the staggered matrix the obtained mean energy resolution was 16% on the top layer and 18% on the bottom layer. The flood maps obtained with the LYSO matrix setup show that the pixels on both the staggered levels are clearly identifiable.

Index Terms—PET instrumentation, Data acquisition systems, Photodetectors.

I. INTRODUCTION

MULTI-MODAL fully integrated Positron Emission Tomography (PET) and Magnetic Resonance Imaging (MRI) have been a main research topic during the last two decades. Since the initial attempts at combining PET and MRI [1], significant development efforts have been put to achieve sequential or simultaneous PET/MRI acquisitions [2].

Pioneering results were achieved by inserting the scintillation crystals inside an MRI system at 0.2 T and connecting them with 3 m long optical fibres to photo-multiplier tubes (PMT) kept outside the magnet [3]. The use of long fibres served to guard the PMTs from the strong magnetic field of the MRI system and to keep the metallic parts of the PMTs

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far from the field of view of the MRI. However, it implied a loss of scintillation light, leading to reduced energy and timing resolution, deterioration in crystal identification and loss of PET signal performance [4]. Other solutions have been proposed in order to keep the PMTs closer to the crystals, such as those based on split magnets [5] or field-cycled MRI [6]. These solutions were usually limited in their magnetic field strength, which in turns limited the MRI performance.

Of the simultaneous PET/MRI acquisition methods that followed, the most common one was based on the PET insert approach, in which a conventional MRI scanner hosted a dedicated MRI-compatible PET system employing avalanche photo-diodes (APD) [7]–[9]. The approach showed to be successful for tumour imaging animal studies and laid the foundation for further developments aimed at brain imaging [10]. With PET inserts based on APDs it was possible to highlight the effects on performance due to the interference with MRI and the importance of a careful shielding. In particular, it was shown that the slight variations of PET energy resolution, time resolution and count rate statistics, when inside the MRI were mostly related to the temperature drifts of the APDs [11].

In 2011, Philips Research presented the first results obtained with a PET/MRI prototype [12] on silicon photo-multipliers (SiPM), a new type of device made of highly integrated arrays of APDs operating in Geiger mode that showed promising characteristics just a few years before [13]. Among their best characteristics SiPMs excel for their high gain and fast time response, which enable sub-nanosecond photon timing resolution and therefore time-of-flight (TOF) PET. In one of the most recent SiPM implementations, the idea of integrating arrays of APDs in Geiger mode was further enhanced by providing the digital logic required to detect and digitize each breakdown on the same Silicon substrate. The resulting device, referred to as digital SiPM, is expected to be unaffected by strong magnetic fields and its intrinsic digitization should make it less prone to electromagnetic interference [14], [15]. Analogue and digital SiPMs represent today the devices at state of the art for photon detection in PET/MRI.

The development of MRI-compatible detectors based on APDs and, eventually, SiPMs, has recently led to the industrial production of simultaneous fully integrated PET/MRI systems for preclinical or clinical imaging [9], [16]–[18]. In particular, PET/MRI showed to be a promising technique for brain studies [19]–[21], and it has generated renewed attention to the development of dedicated PET systems for such applications [22]–

[25]. The dedicated approach for PET offers the advantage of an enhanced spatial resolution and higher sensitivity [26] in exchange for a specialised detector design.

PET detectors that have to be integrated within an MRI must be compact, compatible with strong static magnetic fields and immune to magnetic switching gradients [27]. Depending on the availability of the shielding cases [28], [29], they must also be optimised to reduce radio-frequency interferences [30]. These constraints apply not only to the raw photon detectors, but also to the part of the PET electronics that is placed inside the magnet bore, which we refer to as *front-end*. This part interoperates with the detectors by performing the necessary analogue to digital conversions and transmits the digital data to a central acquisition system that is outside the bore and that we refer to as *back-end*.

The constraints on PET front-end electronics, power supply, power dissipation, encumbrance and data throughput, also reduce the range of available data acquisition architectures. The common approach is to read the photo-detectors with multi-channel application specific integrated circuits (ASICs). These provide the analogue to digital circuitry required to convert the energy and arrival time of the detected gamma photons and transmit them to an acquisition back-end. The ASIC devices available so far may differ in the way they measure the energy, e.g., by converting the pulse peaks [31]–[34], by integrating the current [35], [36], by using non-linear [37]–[39] or linear [40]–[42] time-over-threshold techniques. The technology used for time discrimination may also range from simple or dual thresholds [35], [38] to constant fraction discrimination [43] and more advanced pattern matching [44].

The work presented here is focused on the properties of the specific design choices made in the PET system that is being developed for the TRIMAGE project [45]. The system will make part of a fully integrated PET/MRI/EEG dedicated for brain imaging [46]. In particular, our PET front-end is based on the TRIROC ASIC (Weeroc, s.a.s., Paris, France) [47] which has also been designed within the framework of TRIMAGE. TRIROC uses a simple threshold for time discrimination. Charge measurement is done via pulse peak detection and conversion, while a secondary charge threshold can be enabled for dark noise rejection. The aim is to present the first results that have been obtained with an early prototype of the front-end electronics. Preliminary tests were done by using either single LYSO crystals and LYSO matrices. We will report on the maximum observed event rate, the energy resolution and the coincidence time resolution (CTR) of the prototype. Flood maps were also acquired to assess the pixel identification capabilities.

II. MATERIALS AND METHODS

A. The TRIMAGE PET system

The PET component of the trimodal PET/MRI/EEG TRIMAGE system will consist of 18 segments (detectors) of 54 mm × 162 mm, placed so as to form a ring of 310 mm inner diameter (Fig. 1). The field of view will have a diameter of 240 mm, the expected sensitivity is about 7%. The incoming gamma photons will be digitised and transmitted to a host PC

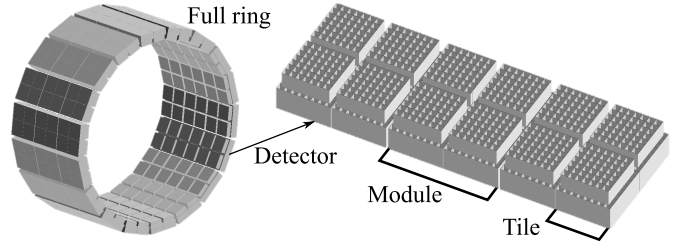


Fig. 1. Picture of TRIMAGE PET detector ring. In the text we refer to a single staggered crystal block and its SiPMs as a tile. A group of four tiles and the electronics to read them is the module.

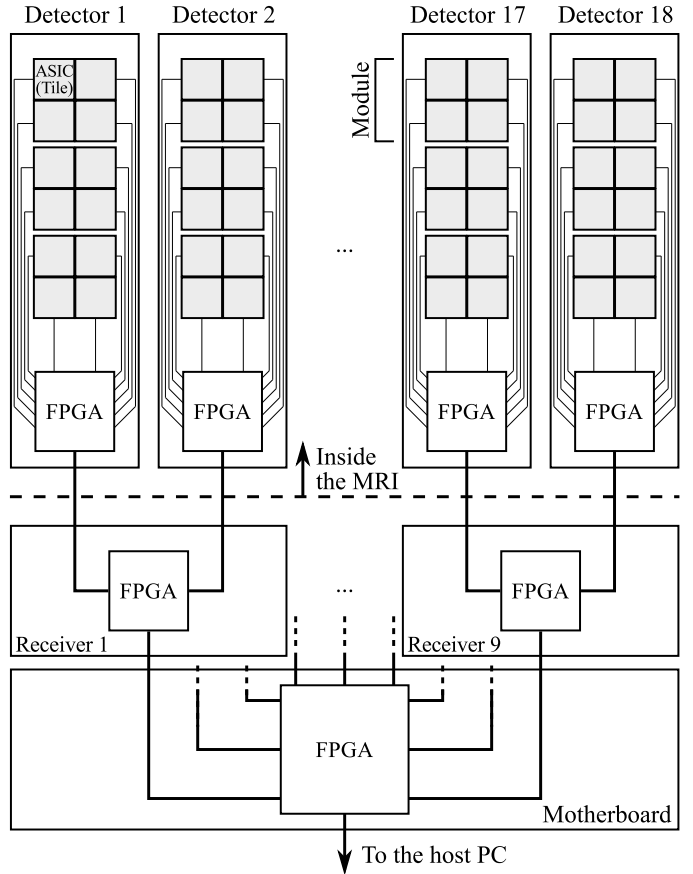


Fig. 2. Schematic diagram of the acquisition pipeline from the ASICs to the host PC. Data is streamed through three multiplexing levels. Only the first level, i.e., the ASICs and the FPGA inside the detector, is going to be placed inside the magnet.

through a processing pipeline divided in three levels: detector, receiver and motherboard (Fig. 2).

The PET detector is based on dual-layer LYSO matrices of 8×8 (bottom) and 7×7 (top) pixels of $3.4 \text{ mm} \times 3.4 \text{ mm}$ pitch. Pixel dimensions are $3.3 \text{ mm} \times 3.3 \text{ mm} \times 12 \text{ mm}$ (bottom) matrix and $3.3 \text{ mm} \times 3.3 \text{ mm} \times 8 \text{ mm}$ (top). Each pixel is wrapped with a 0.1 mm enhanced specular reflector (ESR). The top matrix is optically coupled to the bottom one and staggered by half the pitch (Fig. 3, a) [48], [49]. The free half-entry face of the crystals on the borders of the bottom matrices is covered with a plastic white frame that acts as a reflector.

The crystal pixel pitch was chosen as a compromise between

the intrinsic spatial resolution and the number of channels to read out. The advantage of the staggered configuration is twofold: it allows for a reduction of the depth of interaction uncertainty, as it is limited by the thickness of the layer where the interaction occurs, and it provides a finer sampling of the lines of response with respect to a single layer with the same pixel pitch [50].

The bottom matrix is coupled to two arrays of NUV-SiPMs (AdvanSiD, S.r.l, Trento, Italy) [51]. Each array is composed of 8×4 SiPMs with a sensitive area of $3 \text{ mm} \times 3 \text{ mm}$ and $3.4 \text{ mm} \times 3.4 \text{ mm}$ pitch (Fig. 3, b). The number of microcells per SiPM is 5520. The SiPM array was specifically designed to match the crystal pitch thus providing a one-to-one coupling between the SiPM array and the crystal bottom layer. This solution makes the application of advanced pixel/layer identification algorithm possible [46]. We refer to the assembly of a staggered matrix and its 64 SiPMs as a *tile*.

Each tile is read out by a 64-channel TRIROC ASIC. The maximum power dissipation of the ASIC is 10 mW per channel. The ASIC applies a programmable zero-suppression scheme based on two thresholds, one for enabling the pixels capture and another for enabling the data transmission. Tiles are arranged in groups of four (2×2) and read by four ASICs mounted on a single board (Fig. 4), which we refer to as a *module*.

The acquired data for each SiPM is sparsely encoded, i.e., only the channels that have been triggered inside the ASIC are being transmitted and the redundancies in the timestamps of each single channel are removed.

A 64-bit timestamp is associated to each SiPM channel that crosses the high-gain threshold, i.e., the threshold that is used to provide the fine time measurement. However, only the least significant bits (LSB) of the timestamp are transmitted from the ASIC to the FPGA. The number of bits transmitted per channel can vary according to the following rules: 1) For each channel, the least significant 10 bits are always transmitted (*fine timestamp*, LSB = 24.4 ps); 2) For each channel, the more significant 10 bits are transmitted only if they differ from the previous channel or if it is the first channel to be transmitted of a cluster of channels (*coarse timestamp*, LSB = 25 ns); 3) The 16 more significant bits are transmitted once per event, i.e., once per cluster of channels triggered together (*top counter*, LSB = 250 ns); 4) An additional bit is transmitted along with the top counter to indicate that there has been a counter overflow in the coarse timestamp counter; 5) An additional bit indicates that there has been a top counter overflow. This additional bit pilots a 28-bits wide additional counter running in the FPGA (*global counter*, LSB = 16.4 ms, MSB = 50.9 days). The FPGA combines these data to form the 64-bit timestamps of all the SiPM channels that were triggered.

The FPGA, the three modules, their mechanical support and the RF shield will constitute a *detector*. Most of the data produced from the ASICs will be processed directly by the FPGA inside the detector. Data processing includes on-line pixel identification, energy calibration, timestamping and event packet generation for each incoming gamma photon.

Once generated, the event packets are sent outside the bore to a back-end data concentrator that performs further data

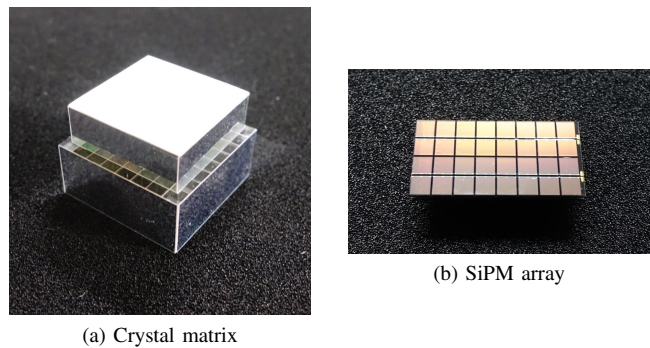


Fig. 3. (a) A dual-layer crystal matrix made of 8×8 LYSO pixels in the bottom layer and 7×7 pixels in the top one. Crystals size is $3.3 \text{ mm} \times 3.3 \text{ mm} \times 12 \text{ mm}$ (bottom) and $3.3 \text{ mm} \times 3.3 \text{ mm} \times 8 \text{ mm}$ (top), with a $3.4 \text{ mm} \times 3.4 \text{ mm}$ pitch. (b) The SiPM array, made up of 8×4 NUV SiPMs ($3 \text{ mm} \times 3 \text{ mm}$ on a $3.4 \text{ mm} \times 3.4 \text{ mm}$ pitch) manufactured by AdvanSiD.

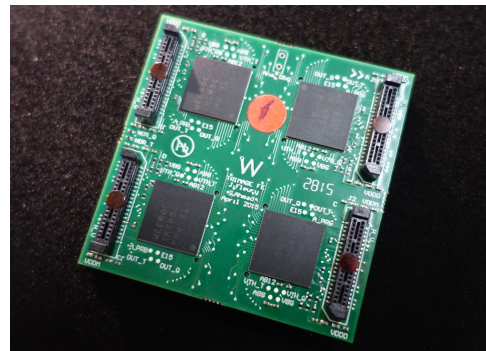


Fig. 4. Picture of the board that hosts 4 TRIROC ASICs. The board allows to read out 256 SiPM pixels and transmits digitally the acquired data to the Altera Cyclone V FPGA.

processing and coincidence detection. In normal operating conditions, the system performs position and energy estimation on-chip and then collects the data in a host PC, in a way similar to [52]. However, the possibility of transmitting all the raw data as in [53] has been kept for analysis and debug purposes.

B. Testing prototype

To preliminary assess the performance of the front-end electronics, a test setup with a single ASIC board was developed. The ASICs are managed by a dedicated system that is functionally identical to the final DAQ electronics to be installed in the TRIMAGE scanner. The system consists of a SoCKit evaluation board (Terasic Inc., Hsinchu City, Taiwan) hosting a 5CSXFC6D6F31C7N Cyclone V System-on-Chip (SoC) FPGA (Altera Corp., San Jose, USA), plus an adapter board and a liquid cooled ASIC board (Fig. 5). Only the ASICs were cooled with water flowing at 18°C . Although the real concern was to keep the SiPMs at a constant temperature, this was considered the most cost-effective solution because almost all the power dissipated close to the SiPMs comes from the ASICs. The SoC hosts an ARM-based Linux operating system, in which the testing and data transmission routines are implemented. The operating system allows to send the acquired data via Ethernet or to store it in a local micro SD memory.

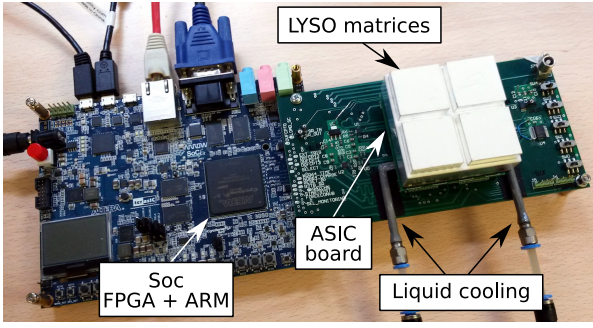


Fig. 5. The data acquisition board hosting an Altera System-on-Chip (SoC) Cyclone V FPGA. The board is liquid cooled. The FPGA on board acquires events from the ASICs and reconstructs the data used for pixel identification.

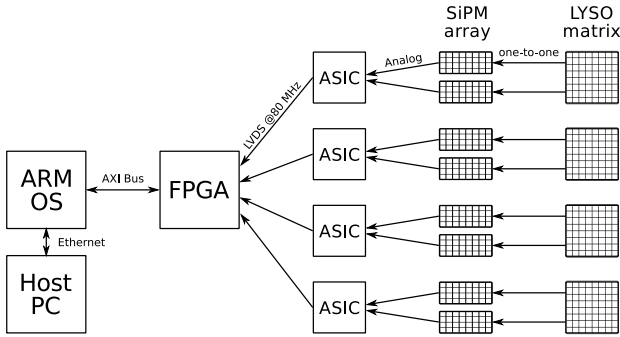


Fig. 6. Block diagram of the data flow from the front-end electronics to the host PC. Data can be stored in the main drive of the operating system running on the ARM processor, or it can be sent to a host PC via Ethernet.

Data is transmitted from the FPGA to the ARM processor via a 128-bit Advanced eXtensible Interface (AXI) bus running at 100 MHz, and from the ARM to a host PC through a Gigabit Ethernet connection. The prototype can be connected to an ASIC board that can readout up to 256 SiPMs with four ASICs. The FPGA provides the ASICs with two clocks, one running at 40 MHz, which is used for the TDC and another running at 160 MHz for serial data transmission. The ASICs in turn transmit one bit of output data every two clock cycles, i.e., at 80 MHz in single data rate. A block diagram of the data path from the SiPMs to the host PC is represented in Fig. 6. It is worth noting that the data path is slightly different from the final version to be implemented for the TRIMAGE scanner, where all the data is multiplexed from 216 ASICs to a central FPGA and from there to a Host PC.

The testing prototype can replicate all the digital functions that will occur in the FPGA, including the data interface with the ASIC. An important difference between the prototype and the final system is that the latter will be able to acquire data from 12 ASICs instead of four only. Another important difference is that the current prototype cannot be used inside an MRI. An MRI-compatible detector with a different physical layout, non-magnetic building materials and proper shielding is still under development.

SiPMs and LYSO crystals can be arranged in the same way as they will be in the final TRIMAGE system. Crystals are coupled to the SiPMs with optical grease.

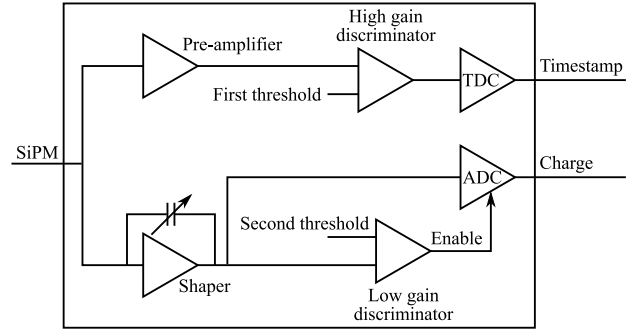


Fig. 7. Simplified scheme of an ASIC channel. The input from the SiPM is split in two paths, one of which is amplified at the earliest stage. The pre-amplified path is referred to as the high-gain (HG) path and it is used for time discrimination. The other one is the low-gain (LG) path, which is used for charge discrimination.

C. ASIC architecture

The TRIROC ASIC architecture is described in detail in [47]. For each channel, the input signal is split into two paths. The high gain path is used to trigger the discriminator and to provide a fine time measurement. Fine time label is recorded when the signal going through the high gain path crosses a programmable threshold (*first threshold* therein). The low gain path is used for event validation and charge to digital conversion. The validation is asserted when the signal going through the low gain path crosses another programmable threshold (*second threshold*). This is the secondary charge threshold that is used for dark noise rejection and that enabled the peak detection. In all our tests, the secondary charge threshold was enabled. A schematic block diagram of the ASIC channel and a time diagram of the signals involved during the conversion are reported in Fig. 7 and Fig. 8, respectively. More details about the internal circuitry of TRIROC can be found in [47]. The digital conversion is performed by a 10-bit Wilkinson ADC at the end of the low gain path. For each event, a series of coarse and a fine time labels is recorded. The coarse time is provided by a free running counter clocked by the TDC clock at 40 MHz; the fine time information is provided by a 10-bit TDC with a time resolution of approximately 40 ps. Digital data is output to five LVDS serial lines running at 80 MHz.

Any new event arriving during the digital conversion is inhibited, i.e., the conversion time can be modelled as a non-paralysable dead time.

D. Firmware

The firmware is structured into five subsystems: 1) ASIC slow control manager, 2) data decoder, 3) event builder, 4) event processor and 5) data transmitter (Fig. 9).

The slow control manages the activation and deactivation of the functionalities of the ASICs, including the activation of the data stream, pedestal readout, and the configuration of the ASIC thresholds and shaper parameters.

Data decoders handle the reception of the LVDS serial data outputs from the ASICs. They perform data deserialization, Gray decoding and reconstruct the timestamps from the coarse and fine time labels. Decoders also perform a stream integrity

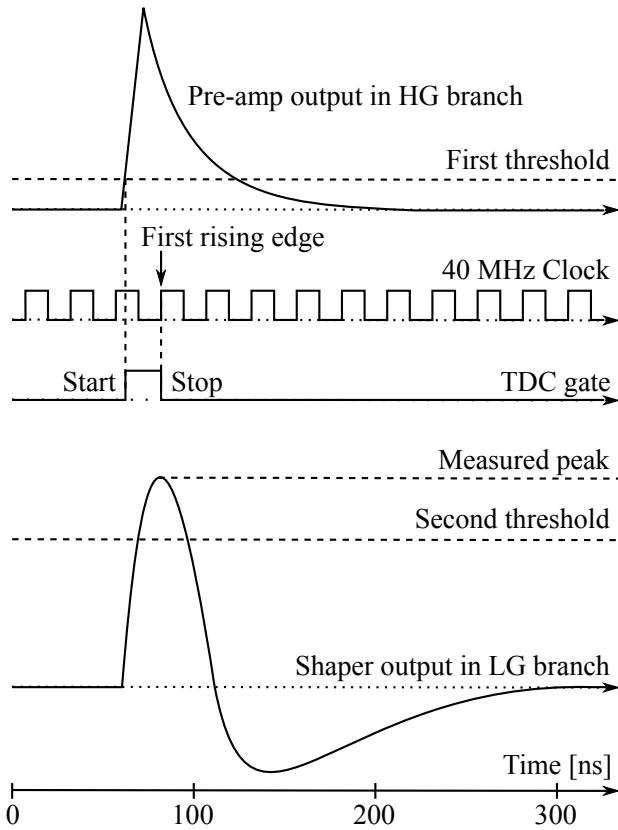


Fig. 8. Time diagram of the signals involved during the conversion. Fine timestamp conversion is triggered when the pre-amp output in high-gain branch crosses the first threshold and stops at the next rising edge of the TDC clock. Peak detection and conversion is triggered when the output of the shaper in the low-gain branch crosses the second threshold.

check. Each data decoder outputs a channel packet for every activated SiPMs, and drives an event start and stop trigger. Channel packets include information on the measured charge, on their timestamp and whether the channel has passed the second threshold. The start trigger is issued when the first channel is received from the ASIC, the stop trigger when the ASIC stops transmitting data. The channels to be transmitted together in a single cluster are decided by the ASIC, which uses a programmable timing window to group channels in clusters. The programmable timing window ranges from 25 ns to 125 ns.

Event builders generate a dense matrix, i.e., a *frame*, with the charge values of all the SiPMs of a full array. All the values are corrected for the mean value of the pedestal, while inactive channels are set to zero. Each cell of the matrix also contains information on the timestamp. The frames produced by the four event builders (twelve in the final version) are then multiplexed and sent serially to an event processor.

The event processor calculates the total deposited energy, the best time estimation and the scintillating pixel. In the current version, pixel identification is obtained by centroid calculation. In this way, also inter-crystal scatter (ICS) events are included. The arrival time assigned to the whole event is the same as the time of the earliest activated channel. No walk correction is currently applied. The event packet is 96 bits

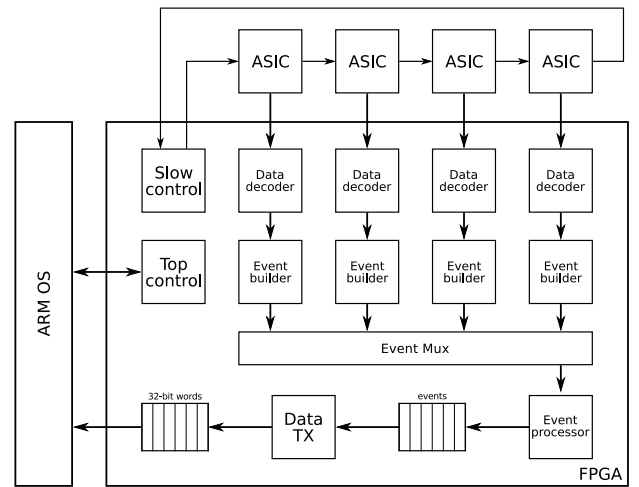


Fig. 9. Block diagram of the FPGA firmware. Data from the ASICs is first decoded then processed event by event and sent to the ARM Linux-based operating system.

wide: 12 bits for energy, 40 bits for the timestamp, 16 bits for the pixel number (which will be unique for every pixel in the whole TRIMAGE scanner) and the remaining bits for control.

The data transmission component allows streaming either all the processed events, which include already the energy, time and pixel id, or the raw data from the data decoders, depending on the user choice. On one hand, transmitting pre-processed data has the advantage of reducing the output data bandwidth by approximately one order of magnitude. On the other hand, transmitting raw data allows performing more in-depth analysis of the ASIC outputs. The second option is necessary to acquire flood maps and generate the pixel id look-up tables (LUT) [53].

E. Experimental setup

1) *Operating point*: The optimal ASIC thresholds and SiPM bias voltage were chosen so as to reject the baseline noise, to have the best detection efficiency and to avoid saturating the ADC dynamic range. A scan of the event rates at different thresholds was performed in the whole bias working range of the SiPMs as specified in the datasheet. The bias voltage and thresholds were then chosen in the following tests so as to work just above the noise level. Only for the coincidence time resolution (CTR) measurements with two single crystals, the ASIC thresholds of the corresponding channels were tuned in order to get the best results.

Room temperature was 23 °C. The ASICs were cooled with water flowing at 18 °C.

2) *Dead time and maximum event rate*: To measure the dead time of the ASIC and the maximum sustainable event rates, we irradiated the LYSO matrices with a ^{68}Ge point source at the distances reported in TABLE I. The activity of the point source was 117 μCi . The measurement has been done by calculating the inverse of the saturation rate, according to the non-paralysable model. The saturation rate has been obtained by estimating the input rate and finding the asymptote of the non-paralysable model fitted on the output rate versus

TABLE I
EVENT RATES VERSUS DISTANCE FROM THE POINT SOURCE.

Distance [mm]	Output rate [Hz]	Estimated input rate [Hz]
20	56 331 ± 81	915453
30	50 993 ± 70	409018
40	45 070 ± 50	231765
50	40 917 ± 56	149723
60	35 965 ± 83	105157
70	31 748 ± 116	78285
120	21 987 ± 158	29191
170	14 595 ± 130	16487
220	11 196 ± 110	11403
270	9218 ± 96	8871
320	7475 ± 90	7430
370	6572 ± 87	6533
420	6050 ± 83	5937
470	5628 ± 82	5520
520	5356 ± 78	5218
570	4992 ± 77	4992
620	4879 ± 74	4879
670	4785 ± 74	4785
720	4624 ± 68	4624
770	4485 ± 66	4485
background	3681 ± 59	3681

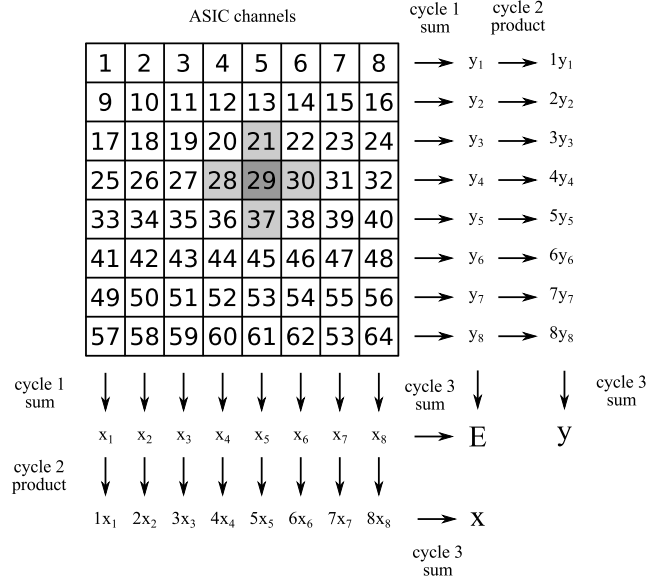


Fig. 10. Centroids are calculated separately for the x and y coordinates as in Anger decoding. The algorithm is parallelized, pipelined and runs at 80 MHz.

input rate curve. Input rates have been estimated under the two following approximations: 1) dead time losses for rates below 5 kHz are neglected, i.e., we assume that the input rate is equal to the output rate when the latter is below 5 kHz; 2) the geometrical efficiency scales with the square of the distance between 20 cm and 95 cm, namely we assume that the input rate decreases with the square of the distance for rates above 5 kHz.

3) *Coincidence time resolution*: For the initial evaluation of energy and timing resolution, two $3.3 \text{ mm} \times 3.3 \text{ mm} \times 8 \text{ mm}$ LYSO scintillator were white wrapped and optically coupled to two SiPMs 13.6 mm apart with an optical grease. A ^{22}Na point source of 544 nCi was placed at the midpoint of the two crystals so as to have coincidences between the two channels. Only events at energies starting from the minimum of the valley before the 511 keV peak were used to reconstruct the CTR. The first thresholds of the ASIC were tuned to get the best results in terms of time resolution. The time resolution obtained this way must be taken as the best case scenario, since it does not include the timing errors due to light sharing and inter-board jitter.

4) *Flood maps*: Flood maps were generated by calculating the 2D histogram of the centroids of each reconstructed frame. The coordinates of the centroids are evaluated as

$$x = \frac{\sum_{i=1}^8 i \cdot x_i}{E} \quad (1)$$

$$y = \frac{\sum_{j=1}^8 j \cdot y_j}{E} \quad (2)$$

$$E = \sum_{i=1}^8 x_i = \sum_{j=1}^8 y_j \quad (3)$$

where x_i and y_j are the sum of the values collected respectively by the i -th column and the j -th row of the SiPM, and E is the sum of the values collected by all the SiPMs.

The actual implementation inside the FPGA, i.e., in the event processor, is illustrated in Fig. 10. The centroid calculation is based on the same principle used in Anger encoding. Centroids are calculated separately for the x and y coordinates. The algorithm is parallelized, pipelined in three stages and runs at 80 MHz. In the first clock cycle, the sum of rows and columns is performed, then, the results are weighted according to each position and, in the third clock cycle, the component calculates the total energy E and the (x,y) coordinates.

Data were acquired with the module irradiated by a ^{68}Ge point source of $72 \mu\text{Ci}$ at a distance of 50 cm. The acquisition was done with the staggered crystal configuration. Starting from the 2D histogram, the crystal centres were identified offline with an automatic blob detection algorithm [54]. Regions corresponding to each crystal were generated using a recursive morphological dilation [46], in which each connected region is assigned a unique grey level and it is grown to fulfil the whole image.

5) *Energy resolution*: The energy resolution was estimated on a single crystal pixel of $3.3 \text{ mm} \times 3.3 \text{ mm} \times 8 \text{ mm}$ and on the whole staggered matrix. In both cases, crystals were irradiated by a ^{68}Ge point source of $72 \mu\text{Ci}$ at a distance of 50 cm. For the acquisition on the staggered matrix, all the crystal gains were equalised using the 511 keV photo-peak as a reference. The spectrum of the whole matrix was evaluated by summing all the gain-corrected energy values. The energy resolution ($\Delta E/E$) is then evaluated as the ratio between the FWHM of the full-energy peak and 511 keV of the energy spectra.

III. RESULTS

A. Operating point

The results of the scan are shown in Fig. 11. The position of the baseline is clearly identifiable on each dataset for thresholds lower than 200 in DAC units. Tests showed that

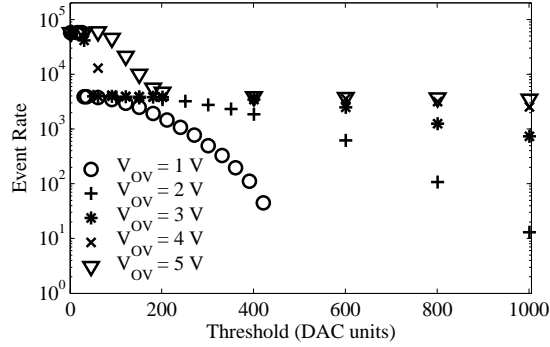


Fig. 11. Event rate measured at different values of the second threshold and at different bias voltages of the SiPMs. The bias voltage spans from 1 V to 6 V overvoltage. The event rate is measured for the whole ASIC. For each event one or more channels can be acquired together.

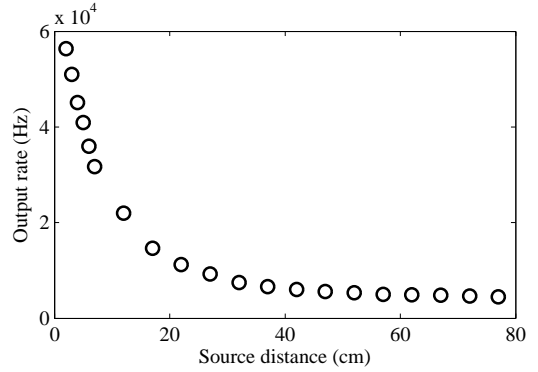


Fig. 13. Output event rates against the distance of the detector from the source. The dashed line represents the fit on the non-paralysable model with a dead time of $(17.2 \pm 0.1) \mu\text{s}$.

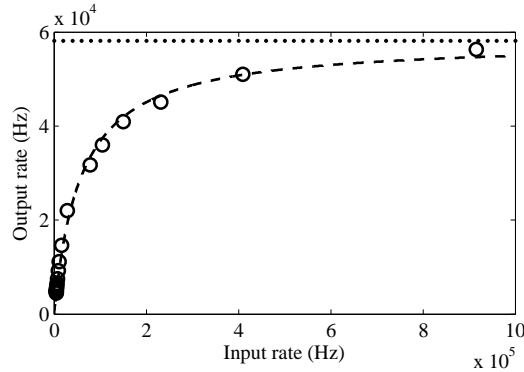


Fig. 12. Output event rates against the input rate from the source at varying distances. The dashed line represents the fit on the non-paralysable model with a dead time of $(17.2 \pm 0.1) \mu\text{s}$. The dotted line at 58 kHz is the asymptote of the output rate obtained from the fit, i.e., the inverse of the dead time.

at a bias voltage of 29 V and with the default parameters for the signal shapers in the ASIC, the photo-peak was well centred in the ADC dynamic range. The validation threshold was set just above the noise level, i.e., at 200 in DAC units.

B. Dead time and maximum event rate

The output rate as a function of the estimated input rate and the distance from the source are shown in Fig. 12 and Fig. 13. The dashed line represents the fit on the non-paralysable model. The estimated value of the dead time is $(17.2 \pm 0.1) \mu\text{s}$, which corresponds to a saturation rate of 58 kHz.

C. Coincidence time resolution

The best CTR obtained with two crystal pixels is $(420 \pm 20) \text{ps}$ (Fig. 14). As expected, The CTR showed to be very sensitive to the value of the first threshold on the high-gain branch of the ASIC.

D. Flood Maps

Two sample light patterns of the optical photons detected in the bottom and top layer are shown in Fig. 15 (a) and (b), respectively. The patterns are very similar to those simulated in previous studies [46].

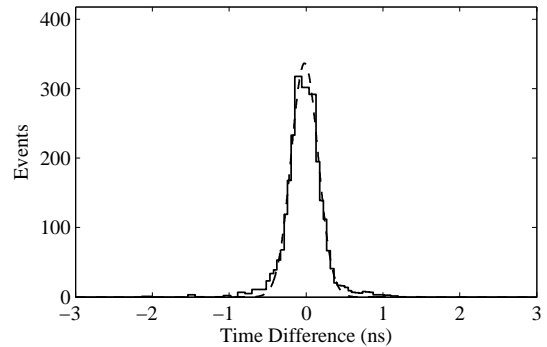


Fig. 14. Coincidence time resolution (CTR) obtained with two crystal pixels. The CTR FWHM is $(420 \pm 33) \text{ps}$.

In the case of events in the bottom layer, the light is mainly concentrated on the SiPM directly coupled with the crystal where the interaction occurs but a significant signal is measured in the channels close to it, too. This effect is due to the optical crosstalk caused by back-reflection of the light transmitted from the bottom layer to the four pixels of the top layer and by the non-negligible thickness of the epoxy resin and optical glue covering the SiPM tile. In the case of a top layer interaction, the light is uniformly distributed on four channels with relatively low light dispersion on the neighbour channels due to a smaller optical crosstalk that, in this case, is due to the SiPM to crystal optical interface thickness only.

A flood map of 200×200 bins obtained with the staggered matrix is shown in Fig. 16 (a). In both layers, crystals are well identifiable. The LUT automatically calculated from the flood map is shown in Fig. 16 (b).

A slight rotation between the crystal matrix and the SiPMs can be observed, which produces a partial loss of information in the edges. In particular, the two pixels in the bottom right corner are partially lost. We think that they can be recovered by correcting the bias and the discriminating thresholds of the corresponding SiPMs, as well as by improving the mechanical precision of the assembly. The regions of the LUT that correspond to those two pixels have been generated by guessing their position to be in a regular grid.

The same misalignment concurs to the double peaks that

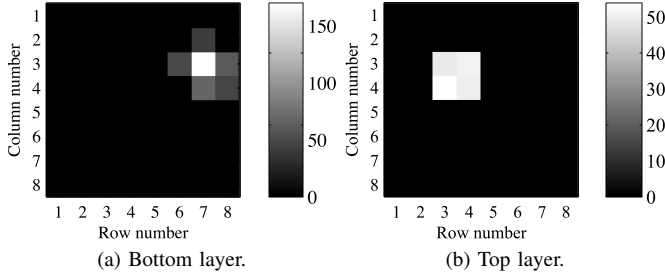


Fig. 15. Example of two light patterns acquired in the staggered configuration. (a) Light pattern produced by the scintillation of crystal (3,7) on the bottom layer. (b) Light pattern produced by the scintillation of crystal (3,3) on the top layer.

can be seen for some pixels. The double peak effect it is expected to be mitigated with a better alignment and a SiPM gain equalisation, which have not been done at this stage.

Thanks to the direct coupling, the LUT is very regular. This indicates that it would be possible to reuse the same LUT for more than one tile and, e.g., to store one LUT per FPGA instead of 12 so as to save on-chip memory.

E. Energy resolution

The energy spectrum of the acquisition on a single pixel is shown in Fig. 17. Since the ASIC has a good linearity in our operating conditions, we converted the ADC output to keV by subtracting the pedestal value and scaling directly the photopeak to 511 keV. The energy histogram shows a resolution of 10.7% at 511 keV. This value is not corrected for the SiPM saturation. This effect might be significant in this case due to the one-to-one coupling causing an underestimation of the FWHM of the full energy peak. The mean energy spectra for the top and bottom layers of the staggered matrix are shown in Fig. 18 and Fig. 19, respectively. The conversion to keV has been done as for the single crystal. The obtained energy resolution at 511 keV is 16% for the top layer and 18% for the bottom one. Although not corrected for the SiPM saturation, these values are more realistic than the energy resolution measured with one pixel only because of the smaller signal per SiPM that is recorded when using the staggered configuration. The worse energy resolution of the bottom layer can be attributed to the higher light dispersion occurring when the scintillation light is produced in the bottom layer that makes more likely to lose the information on the neighbour channels, which may not reach the first threshold on the high-gain path of the ASIC. This effect also contributes to the distortion of the energy spectrum at low energies. In fact, the lower the energy is deposited in the bottom layer the higher the fraction of lost light is. As a consequence, there is an excessive fraction of events in the energy spectrum below about 200 keV.

IV. DISCUSSION

The proposed system is characterised for performing an early digitisation of the incoming annihilation photons as in [12], [53], [55] and in opposition to other approaches where

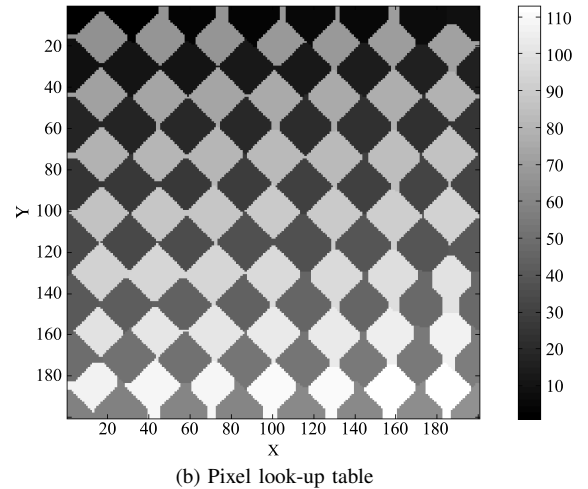
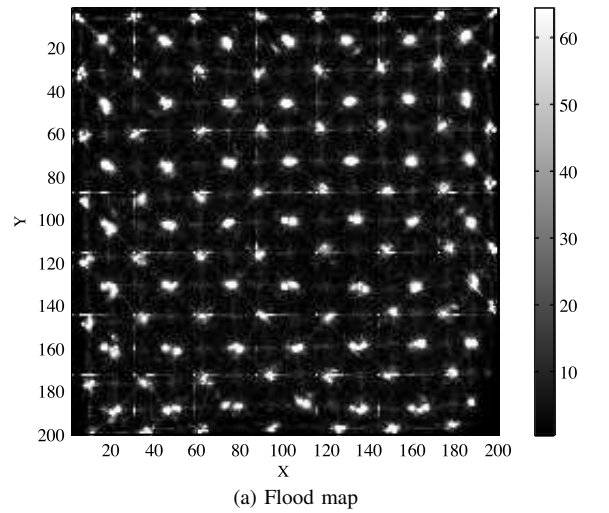


Fig. 16. Flood map (a) and pixel look-up table (b) obtained in the staggered matrix configuration. In the look-up table, pixel numbers are mapped to gray colors from 0 (darkest) to 112 (lightest). Pixel numbers 0 to 63 belong to the bottom layers and 64 to 112 belong to the top layer.

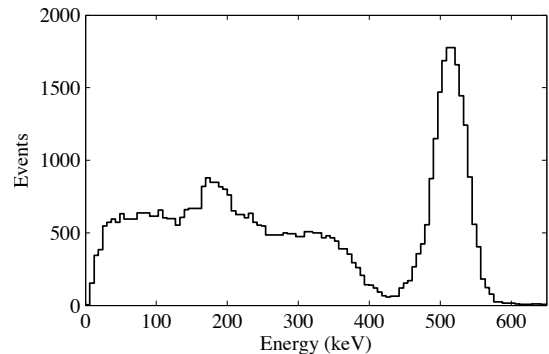


Fig. 17. Energy resolution acquired with a single LYSO crystal of $3.3 \text{ mm} \times 3.3 \text{ mm} \times 8 \text{ mm}$. The obtained resolution is 10.7% at 511 keV.

the analogue signals are transferred to the back-end [21]. Moreover the proposed system performs also pixel identification, energy correction and timestamping in the front-end in order to optimise the data bandwidth of the cables from inside the magnet to the outside. This is different from [12], [53],

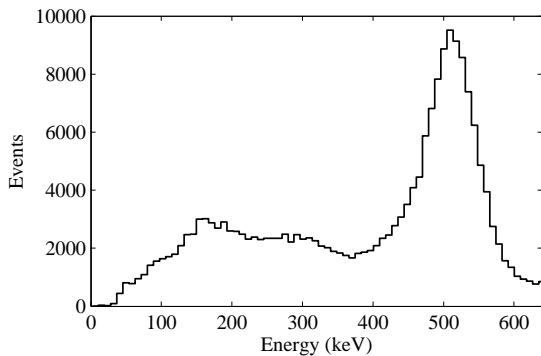


Fig. 18. Mean energy spectrum acquired on the top layer of the staggered matrix. The energy resolution is 16% at 511 keV. An energy cut was set to 650 keV by software in the automatic energy calibration procedure.

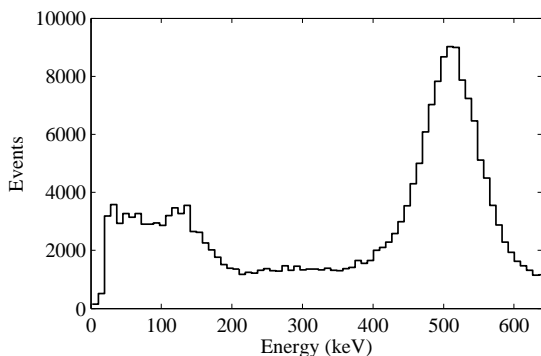


Fig. 19. Mean energy spectrum acquired on the bottom layer of the staggered matrix. The energy resolution is 18% at 511 keV. An energy cut was set to 650 keV by software in the automatic energy calibration procedure.

[55], where this kind of processing is performed software-wise by a central unit in the back-end.

Another unique feature of the system is the combination of a dual layer staggered matrix with a one-to-one SiPM to crystal coupling at the bottom layer. This characteristic provides robust pixel identification and DOI capabilities.

Initial tests have shown that pixels and layers can be well distinguished, suggesting that the final system will be able to fully exploit the benefits of the staggered crystal configuration, i.e., the reduction of the depth of interaction uncertainty and a finer sampling of the lines of response.

Further work will be dedicated to explore the possibility to include more advanced pixel/layer identification algorithms and ICS rejection strategies as suggested in [46].

The saturation rate of TRIROC resulted to be 58 kHz, which is compatible with the maximum expected input rate for the TRIMAGE target brain applications, i.e., 20 kHz per ASIC.

By tuning the high-gain threshold, the low-gain threshold and the input impedance we achieved a CTR of 420 ps FWHM with a couple of single crystals. Although we feel that there is still room for improvement regarding the CTR, by a finer tuning of all the TRIROC channels, this result is already compatible with non-TOF applications.

V. CONCLUSION

We have developed a data acquisition system for early prototyping of the SiPM readout with the TRIROC ASIC. Basic performance of the TRIMAGE PET detector, such as pixel/layer identification, energy resolution, dead time and coincidence time resolution were evaluated. This paper demonstrates the possibility to perform real-time calculations on the SiPM output frame at the level of the front-end FPGA.

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