

Advances in Li-Ion Battery Management for Electric Vehicles

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Abstract—This paper aims at presenting new solutions for advanced Li-Ion battery management to meet the performance, cost and safety requirements of automotive applications. Emphasis is given to monitoring and controlling the battery temperature, a parameter which dramatically affects the performance, lifetime, and safety of Li-Ion batteries. In addition to this, an innovative battery management architecture is introduced to facilitate the development and integration of advanced battery control algorithms. It exploits the concept of smart cells combined with an FPGA-based centralized unit. The effectiveness of the proposed solutions is shown through hardware-in-the-loop simulations and experimental results.

I. INTRODUCTION

The traction battery is undoubtedly the most challenging component in an electric vehicle (EV), as it mainly contributes to set EV performances, especially the driving range and costs. Li-Ion battery technology, with its continuous improvement in energy density and cost reduction, is becoming the battery of choice for the EV traction battery. Its performance and safety, however, strongly depend on an appropriate control of the battery charging/discharging processes, which are carried out by the Battery Management System (BMS) [1].

Although a great deal of research has been conducted to improve the BMS functionalities, especially State-Of-Charge (SOC) and State-Of-Health (SOH) estimation [2], [3] and cell balancing [4], [5], further research efforts are needed for better utilization of the battery energy and power and to meet the strict safety requirements required by the upcoming autonomous driving vehicles [6], [7]. Moreover, with the reduction of Li-Ion cell costs, the impact of the BMS and the battery assembly on the overall battery system cost is becoming more and more relevant. This demands advanced BMS algorithms for more accurate and reliable control of the battery operation, as well as, new solutions for their effective hardware implementation [8]–[10].

Some works in literature have already introduced the concept of Smart Cell (SC) [11]–[14]. It is based on the combination of a Li-Ion cell and an electronic circuit with a microcontroller, embedded in a single case. The microcontroller allows the cell to execute some simple operations, like data acquisition and basic data processing, and to communicate with a master BMS unit.

The performance of Li-ion batteries is highly dependent on their temperature. The higher the temperature, the more

efficient the battery operates (due to smaller internal losses) [15]. However, battery degradation also accelerates with temperature [16]. This makes accurate estimation and prediction of the temperature essential for a good balance between battery efficiency and degradation. In addition, extreme usage (fast charging, high EV acceleration or deceleration processes) could result in the battery temperature exceeding its safe operating range, leading to operational safety risks.

In automotive applications, where high reliability and low costs are demanded, thermistors are commonly used for temperature measurement of the battery cells. However, the main drawback of using thermistors is their placement on the outer surface of the battery case. The accuracy and the dynamics of the cell temperature measurement, especially for detecting peaks or overload, is mainly influenced by the thermal coupling between sensor and cell, as well as by the thermal capacity of the electrode stack and housing. Temperature differences of 10 °C and above between the cell surface and its core have been reported [17]. It follows that, to guarantee safe operation of battery cells within battery packs, monitoring cell core temperature is needed. To insure efficient and safe battery operation, cell core temperature is needed both for present values (estimation), as well as for future values (prediction).

The aim of this paper is to present new and effective BMS solutions for accurate and reliable battery monitoring and control, with special focus on the crucial temperature parameter. A new solution for sensorless temperature measurement and the concept of SC are discussed in Section II, while the development of a core Temperature Prediction Algorithm (TPA) is described in Section III. To foster the adoption of the SC concept and the introduction of advanced battery control algorithms, a field-programmable-gate-array (FPGA) system on chip based hardware/software platform for implementing a master BMS is presented in Section IV. The effectiveness of the platform is shown through the software implementation of the TPA and the Adaptive Mix Algorithm (AMA) [10] as a hardware accelerator.

II. ONLINE SENSORLESS TEMPERATURE ESTIMATION

A. Smart Cell with impedance based sensorless temperature estimation

To overcome the limitations of using thermistors for battery temperature monitoring, the impedance based sensorless tem-



Fig. 1. Smart battery cell integrated on a prismatic BEV4 size battery cell with fully integrated battery monitoring and impedance based temperature estimation (SMD components on bottom side).

perature estimation has been proposed and a circuit has been developed [13]. In comparison to Electrochemical Impedance Spectroscopy (EIS) measurements, which use a wide excitation spectrum [18], the single frequency measurement can be tuned for online implementation into any kind of EV, stationary systems or aviation applications. It has been shown that the excitation frequency can be optimized for low SOC dependency, highest noise immunity and sufficient inner cell temperature dependency [13].

Previous developments have led to a smart cell electronics that has been integrated on a prismatic BEV4 size lithium-ion battery cell (Fig. 1). This electronics comprises main functions as cell voltage reading, capacitively coupled communication to the BMS master, passive cell balancing, conventional temperature sensor reading and the impedance based temperature estimation. It uses a Cypress PSoC5LP MCU for cell excitation control, data acquisition and data processing and is adopted for the implementation of the described sensorless temperature estimation.

B. Sensorless Temperature Estimation Implementation

The sensorless temperature estimation circuit uses a single frequency galvanostatic excitation with a current offset, thus the current varies between 0 and I_{peak} . The circuit allows for two different excitation modes:

- Pure analog sine wave excitation through a DAC and a FET driven current sink: The DAC may set a voltage of up to 1 V over the 150 m Ω current sense resistor.
- PWM modulated sine signal with high frequency control. The current limit is achieved by a current limiting resistor.

For a temperature measurement each second, the excitation current is applied to the cell for 20 ms (20 periods at 1 kHz excitation frequency) and the voltage response as well as the current signal is sampled synchronously. The implemented Goertzel algorithm is used to calculate phase and amplitude of the signals [19]. This could be either done on the MCU of the SC or the samples are send to a host PC for visualization purposes. By applying digital filters, the measurement results can be further processed if needed.

Finally, the phase information is converted to an equivalent cell temperature through a modelled cell phase dependency on temperature and SOC [13].

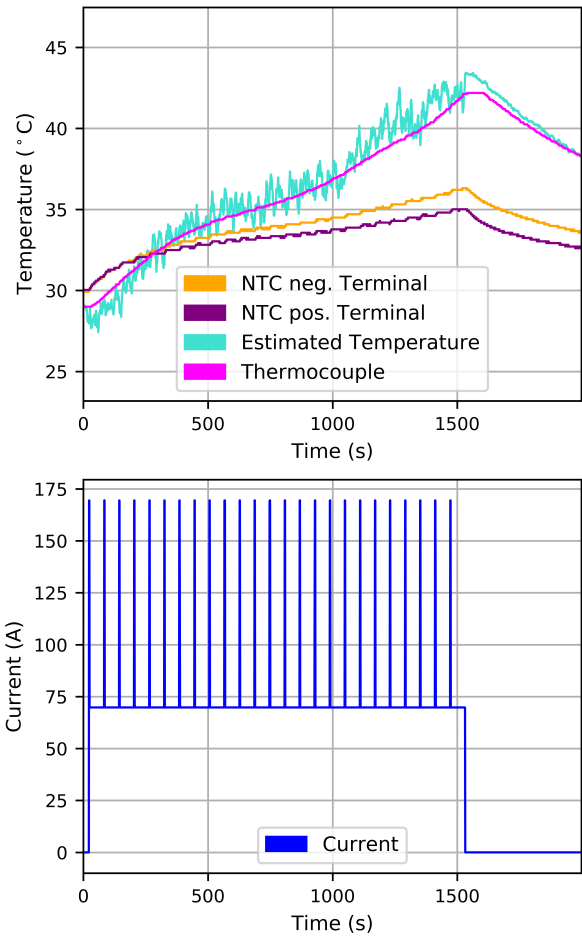


Fig. 2. Sensorless temperature estimation results obtained on an approximately 34 A h prismatic lithium-ion battery cell during pulsed discharge.

C. Algorithm Validation

The previously described calibration process and algorithm was applied to an approximately 34 A h prismatic NMC lithium-ion battery cell. This battery cell was modified during the manufacturing process by adding a thermocouple to the center of the jelly roll. This special construction made a precise validation of the concept and algorithm possible.

The validation process was performed as follows: the cell was placed inside a thermal chamber and connected to the previously described sensorless temperature estimation circuit. The internal thermocouple was connected to this board as well as two NTC sensors, which were placed on the cell terminals. By placing the sensors on the terminals, the measurement results are comparable to readings performed in commercially available EVs, where the temperature sensors are usually placed on the busbars (e.g., BMW i3). The battery cell was then discharged by a 70 A (approximately 2 C) discharge current that was increased to 170 A (5 C) each minute for 2 s, till the cell reached its discharge voltage limit. Fig. 2

shows the experimental results. The lower figure shows the cell current whereas the upper figure shows the three measured temperatures and the estimated inner cell temperature.

It is clearly visible that the measurement of the cell terminals does not give a precise estimation of the inner cell temperature that has been measured by the built-in thermocouple. Although the estimated cell temperature shows some noise, it clearly follows the inner cell temperature. This enables a more precise estimation of the battery state and less cell temperature driven derating of the maximum battery current. In an EV application, less current derating means either a smaller battery and thus cost reduction, or better driving dynamics and performance.

III. TEMPERATURE PREDICTION ALGORITHM

To predict battery core temperature, a future load profile prediction algorithm is combined with an equivalent circuit battery electro-thermal model, describing both battery surface and core temperature. To insure the predictions are accurate over the lifetime of the battery, as its behavior changes, algorithms that estimate relevant parameter variations are included.

Load cycle prediction has been addressed in the past, for a wide range of automotive applications. In [20], complete drive cycles are predicted using a stochastic approach, based on Markov chains. While the method is applied for deriving representative cycles for laboratory/test-bench vehicle testing, this can be adapted to provide online prediction of the future vehicle drive cycle.

In [21], shorter term prediction horizons are addressed, to provide dynamic battery limitations for electric machine control, such as maximum charging or discharging power. The prediction employed here is much simpler, based on battery current, power and voltage limitations.

Equivalent circuit modelling has been widely used in the past to describe electro-thermal behaviour of batteries [15], [17], [21]. Computationally efficient, it is a fast enough method for inclusion in BMS algorithms. This is achieved at the expense of spatial resolution (these models represent average values per cell). To accommodate for these limitations, the electro-thermal model presented in this work increases the spatial resolution by incorporating core temperature.

A. Algorithm Description

Fig. 3 provides an overview of the TPA structure. Battery measurements (current, voltage and temperature) are used to:

- Predict the future load cycle of the battery over a given prediction horizon (block 1); a user defined time horizon is used for the prediction;
- Estimate the current electro-thermal battery model parameters (block 2); past data are used to update the electro-thermal model parameter estimates.

This information is then used by an electro-thermal battery model (block 3) to predict the battery temperature (surface and core) over the given time horizon.

An equivalent circuit approach is followed for the electro-thermal model. This allows for computational efficiency of the

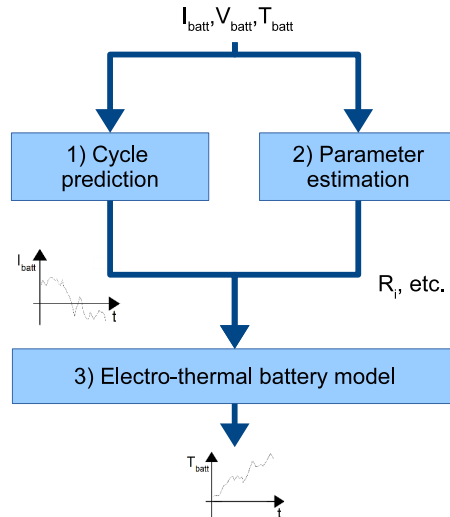


Fig. 3. Thermal prediction algorithm diagram.

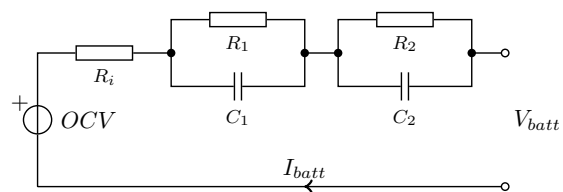


Fig. 4. Electrical battery model - equivalent circuit approach.

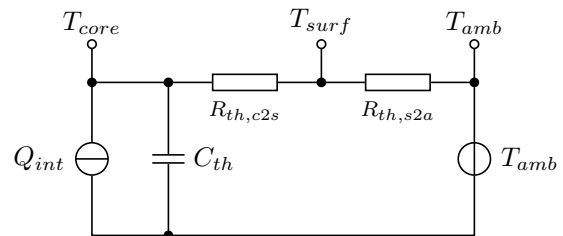


Fig. 5. Thermal model - equivalent circuit approach.

online implementation, as well as online parameter adaptivity. The electrical and thermal models are presented in Fig. 4 and Fig. 5, respectively. It should be noted that the 2 models are coupled: the electrical inefficiencies (power dissipated over R_i , R_1 and R_2) determine the heat generation of the thermal model, while the temperature affects the parameter values of the electrical model. The thermal model describes both surface and core temperature, and uses two thermal resistances to describe the heat exchange between core and surface. $R_{th,s-c}$ [K/W] describes the heat resistance between core and surface, while $R_{th,s-a}$ [K/W] the heat resistance between surface and ambient.

The future load cycle prediction calculates the expected

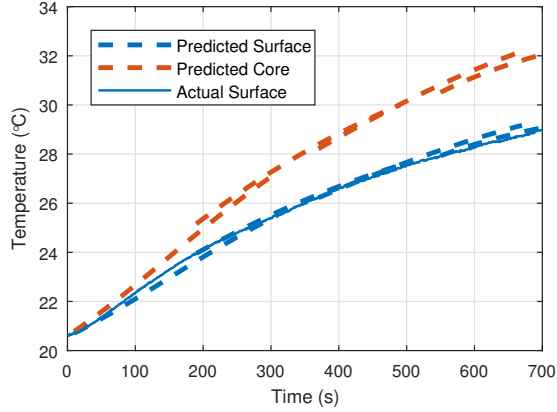


Fig. 6. Temperature prediction paths.

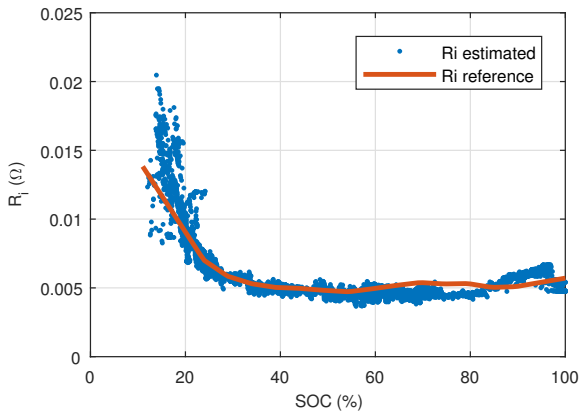


Fig. 7. Internal resistance online adaptivity.

current profile over the given prediction cycle, while the parameter estimator block determines the current value of the electric circuit parameters influencing heat generation.

B. Algorithm Validation

Fig. 6 presents the results of the temperature prediction algorithm, applied to a pouch battery cell tested in a thermal chamber. The cell surface was measured, while the algorithm predicted both cell surface as well as core temperature. For this case, the prediction window was 300 s. The prediction was repeated every 200 s. It is visible that overall, the surface temperature prediction matches well with measured data. The thermal resistances between core and surface and surface and ambient identified for this cell are shown in Table I.

The algorithm predicts up to 2.5 °C temperature difference between the core and surface for this application. This value, smaller than reported elsewhere [17], is due to the type of cell used here: a flat pouch cell. As shown in Table I, the thermal resistance between the core and surface is smaller than the thermal resistance between surface and ambient, indicating a rather homogeneous inner cell temperature. It should be

TABLE I
CELL THERMAL MODEL: IDENTIFIED PARAMETERS

Parameter	Value	Unit
$R_{th,s-c}$	0.32	K/W
$R_{th,s-a}$	0.98	K/W
C_{th}	351	J/K

considered that the thermal resistance to ambient will vary depending on the surrounding of the cell, based on the thermal design of the pack. Because of this, it is important to identify the thermal resistances in the relevant battery operational environment.

The battery internal resistance determines the heat generation within the battery. As the internal resistance increases as the battery ages [16], so will the internal heat generation within the battery. To track this behaviour over the lifetime of the battery, an online estimation algorithm for the internal resistance is included here [22]. Results are shown in Fig. 7, where the algorithm estimates of R_i , during an automotive driving cycle (blue dots), are compared with reference values for the same cell, obtained from hybrid pulse power characterization test profiles. Results show good agreement between algorithm estimates and laboratory tests.

IV. DESIGN OF THE FPGA-BASED SYSTEM ON CHIP BMS PLATFORM

Many BMS architectures have been presented in literature which differs in the distribution of the various functionalities among different hierarchical levels depending, for example, on the choice of the balancing technique and the organization of the battery pack [23].

A centralized architecture, in which all the functionalities are localized in a single board, is a simple and cheap solution. However, it is suitable only for batteries with a low number of cells and is characterized by a low scalability. On the contrary, a distributed architecture is more flexible and scalable to the despite of costs and complexity. Here the functionalities are divided between a central unit (master) and local circuits that usually control groups of cells (slaves). The master unit is usually based on a microcontroller that executes the control and the state estimation algorithms using the data received from the slaves. The latter perform the measurement of the cell voltages thanks to dedicated chips (*i.e.*, stack monitors) able to manage a limited group of cells (*e.g.*, a module composed by 12 cells) and to communicate the acquired information to the master unit, usually in a daisy-chain structure.

A. BMS Architecture

Hereafter, a novel distributed architecture based on a system on chip as master unit is presented. The block diagram of the system is shown in Fig. 8. In particular, the used device is composed by a dual-core ARM[®] Cortex[™]-A9 processor flanked to the FPGA fabric. The slaves are the SCs, which are able to perform simple operations and to communicate

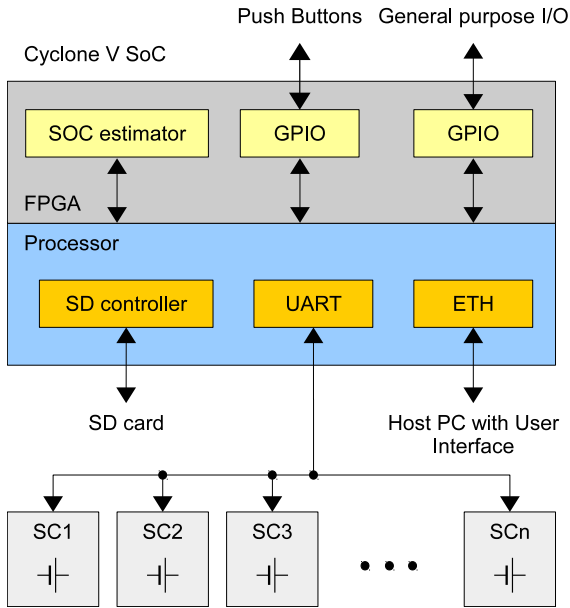


Fig. 8. Block diagram of the proposed BMS architecture based on a system on chip as main unit which manages a certain number of Smart Cells (SCs).

some information to the master unit, by using a serial communication bus. The SCs can indeed measure their voltage, current and temperature, to activate a balancing mechanism, when required by the master unit, and also to provide some status flags in order to quickly detect faults, like over and under-voltage conditions.

The main advantages of this solution are the high flexibility and modularity, as well as the possibility to execute very complex algorithms thanks to the available computational power of the system on chip. In fact, the master unit computes the state of all the SCs by executing advanced algorithms that can be accelerated in hardware. The hardware acceleration allows the system to work in batteries with a large number of cells since the estimators can be employed in time division multiplexing for all the cells. The input of the estimators are the data collected by the communication bus. All this information is used to manage the battery power flow and to optimize the battery usage by managing each single SC.

B. Master Unit

The master unit is based on the Intel Cyclone[®] V system on chip 5CSEMA5F31C6N device, mounted on the DE1-SoC development board. The FPGA fabric allows the system to use reconfigurable peripheral which are needed for low latency and high throughput. The hardware modules are managed by the processor together with the others tasks of the BMS. The processor executes a Linux Ångström distribution, equipped with a real-time kernel. Several processes are executed on boot time, one for each functionality of the BMS. These processes are developed as clients that communicate with a server application. The latter manages the data exchange by using the Unix Socket paradigm. The modularity of the

software structure allows the developer to easily add or update new functions to/in the BMS.

C. Hardware/Software Partitioning

An important development phase is the hardware/software partitioning of the functionalities. In this work, the control strategies and some estimation algorithms are implemented in software. The system is provided with a dedicated client for the communication with the SCs by using the serial interface, a client to manage the user interfaces and the logging of the information in the SD card and one for the activation of the balancing function and the control of the protection switch through the general purpose I/O (GPIO) pins.

Each client application executes a series of standard functions in order to activate the connection with the server process and to exchange data with it. The developer can easily use the obtained data to run the algorithm described in C language. Then, the executable file can be built and loaded in a dedicated folder of the SD card, adding its name in the list of applications that will be executed on operating system boot.

Other important clients are those that communicate with the hardware peripherals. These clients embed the task to send the inputs and to read the outputs from the FPGA fabric by using a Memory Mapped (MM) interface. In fact, each peripheral is provided by a set of registers used by the processor to write and read information. In this work, the FPGA fabric is used to manage various general purpose I/O pins and to implement a hardware module for the SOC and battery parameters estimation.

The developer can integrate into the system already available Intellectual Properties (IPs) or develop a custom hardware module by using a HDL description, assuming that they are provided with a MM interface.

D. Validation of the Implemented Platform

The TPA and the AMA have been implemented on the proposed platform in order to show its capabilities. The first algorithm is implemented in software by following the procedure described in the above Section, and it used to predict the core temperature of each cell. On the contrary, the AMA is implemented as a hardware module by using a high level description of the algorithm, as shown in [10]. It is a model-based technique, which combines the Mix Algorithm [24] for the SOC estimation and the Moving Window Least Squares (MWLS) method [25] for the online identification of the cell model parameters.

The platform has been tested with the set-up reported in Fig. 9, by simulating the battery usage in an automotive environment. As said above, the master unit is represented by the DE1-SoC development board. It is connected to a host PC by using the Ethernet interface. This communication link is used to send all the acquired and computed data to the user interface implemented in LabVIEW and enable the visualization and memorization of this information. The behaviour of a battery composed of a certain number of SCs is emulated by using a SC emulator that reads all the cell

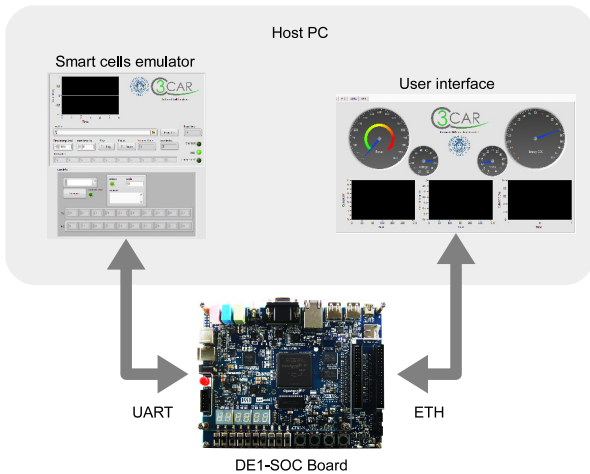


Fig. 9. Block diagram of the experimental set-up.

data from a text file. In particular, in this work, the emulator simulates 12 physical SCs and communicates with the master unit a UART link.

The text file contains the current and voltage profiles of the battery cells, which are representative for a battery used in an EV driven in an urban environment: the Urban Dynamometer Driving Schedule (UDDS). In particular, the battery starts the test with an SOC equal to 80% and the UDDS cycle is repeated until the SOC reaches the value of 20%. These profiles (see Fig. 10) are generated by using a battery model [9] including a thermal description of the cells. The electrical part of the battery model is also used to generate the reference values of SOC and model parameters shown in Fig. 12, while the thermal one allows us to have a reference for the core temperature prediction, as drawn in Fig. 11.

Fig. 11 shows the temperature predicted by the TPA for one of the 12 simulated SCs. In this case, both the prediction window and the prediction update interval are 100 s. From the graph, it is visible that the predicted temperature is coherent with the simulated one.

The results of the AMA are shown in Fig. 12. The estimated SOC is in good accordance with the simulated one, resulting in an rms error of 2.8%. Very good results are also achieved in the estimation of the series resistance R_i and the time constant $\tau_1 = R_1 C_1$, even if the latter is more noisy because the battery model response is less sensitive to this parameter [26]. This information is very useful in the estimation of the SOH variable, since it is linked to the value of the internal resistance [27].

V. CONCLUSIONS

This paper has presented some advanced battery management solutions aiming at a better and safer use of Li-Ion batteries in EVs. In particular, a new and easy to implement method for sensorless temperature measurement has proven to be capable of monitoring the core temperature of a battery cell. This enables a less cautelative use of the battery, in terms of

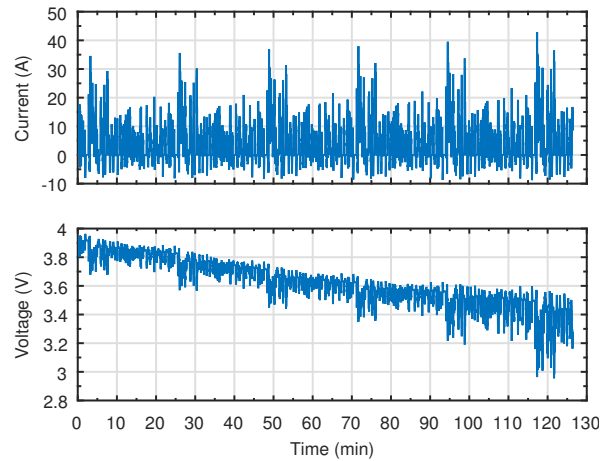


Fig. 10. Cell current and voltage profile in five consecutive UDDS cycles.

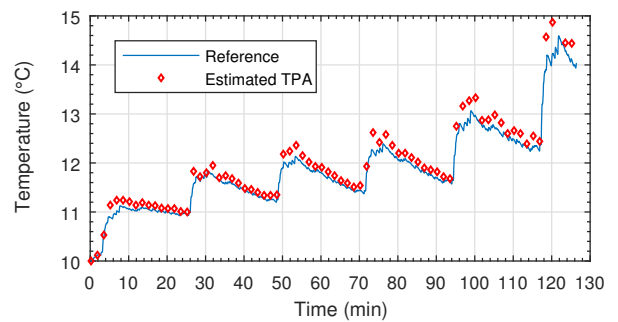


Fig. 11. Comparison between the simulated and the predicted cell core temperature.

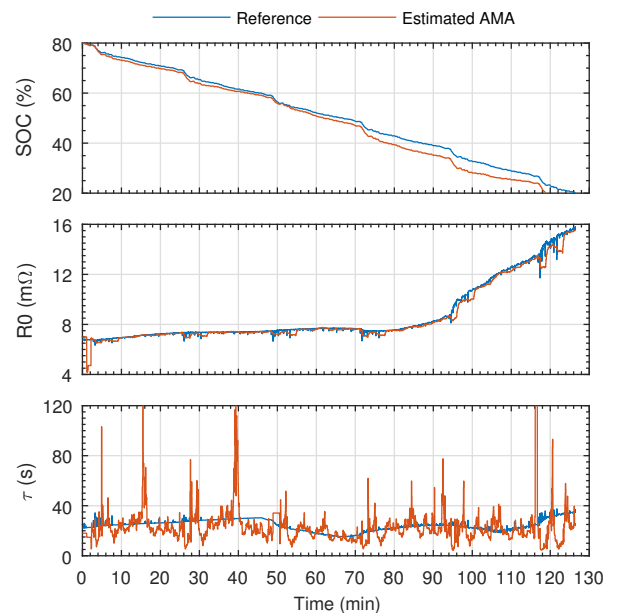


Fig. 12. Comparison between the simulated and the estimated cell SOC and model parameters for one of the twelve cells in the emulated battery pack.

delivered power, while preserving or even increasing the safety level. Further improvements can be achieved by adopting the TPA, which makes it possible to estimate the cell core temperature trend and, thus, a more effective control of the battery operation. Finally, a hardware/software platform based on an FPGA system on chip solution has been introduced and validated for fast development and integration of advanced battery control algorithms, such as the TPA and AMA for cell core temperature prediction and SOC estimation. The developed platform smoothly combines with SCs, in which the electronics integrated in the cell carries out simple monitoring tasks, such as the proposed sensorless temperature measurement, while the platform enables the execution of advanced algorithms in parallel on all the battery cells through hardware acceleration.

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