Pixel design driven performance improvement in 4T CMOS Image Sensors: Dark Current reduction and Full-Well enhancement

Alessandro Michel Brunetti, *Member, IEEE*, Mattia Musolino, Sebastiano Strangio, *Member, IEEE*, Bhaskar Choubey, *Senior Member, IEEE*

***Abstract*—Dark current limits the optical performance of CMOS image sensors. The main sources of the dark current in a modern submicron process are the defects induced by the shallow trench isolation fabrication process steps. In this paper, we present a pixel layout technique to reduce the impact of these defects by removing the trench-oxide between the two adjacent edges of neighbouring photodiodes. This isolation scheme relies on the p-well layer only and provides the further advantage of requiring less area. Hence, a larger photodiode can be designed, leading to an increased pixel fill factor. Experimental results show that this approach reduces the dark current by 21% and increases the linear full well capacity by approximately 9%.**

***Index Terms*—CMOS Image Sensors, Pixels, Dark Current, STI, Full Well, Layout.**

I. Introduction

CMOS image sensor (CIS) is one of the fastest growing sectors for consumer electronics [1]. The increasing need for improved performance is calling for continuous device optimisation [2][3][4][5] aimed at counteracting the effects of the parasitic phenomena. The dark current (DC), for instance, is one of the principal causes of image quality degradation at low light due to thermally-generated leakage currents in the photodiode (PD) [6][7][8][9][10][11].

From a manufacturing process point of view, there are several effective ways to reduce the DC [9]. As regards the DC originating at the silicon surface, it can be reduced by hydrogen annealing [12], fluorine passivation [13], multi-pinning layers [14] and double buried charge channels [15]. On the other hand, the DC induced by the lateral isolation can be reduced by a variety of barriers between the active area and the isolation scheme [7][8][16].

Manuscript received May 15, 2019. This work was supported by the EU FP7 Marie Curie Programme and by the project EDISON-GA under Grant 317497.

A. M. Brunetti was with the University of Oxford, Oxford OX1 3PJ, U.K, and he is now with Caeleste, Mechelen, 2800, Belgium (phone: +32488809278; e-mail: alebrune@gmail.com).

M. Musolino is with LFoundry, a SMIC Company, 67051, Avezzano, AQ, Italy (e-mail: mattia.musolino@lfoundry.com).

S. Strangio is with the Dipartimento di Ingegneria dell'Informazione, Università di Pisa, 56122, Pisa, Italy (e-mail: sebastiano.strangio@unipi.it).

B. Choubey is with the institute of analogue circuits and image sensors, Siegen University, 57076 Siegen, Germany (e-mail: Bhaskar.Choubey@uni-siegen.de).

The aforementioned optimisation approaches are generally very costly and often are not available to most designers, since they involve modifications of the fabrication process. This has led to many studies to reduce the DC that can be applied at the design/layout level without changing the operation scheme of the pixel [17][18][19][20]. These approaches usually aim to avoid the interaction of the Shallow-Trench-Isolation (STI) with the PD, thereby reducing the defects induced leakage current. Guard rings made of polysilicon or p-well have been suggested to suppress the formation of the STI layer around the PD [21][22]. Techniques like ring-gate shared pixel design enclosed by p-type layers, have also been proposed [10]. Choi et al. have suggested a hybrid STI/p-well isolation scheme to achieve low leakage [23], which was benchmarked against the STI and the pure p-well isolation techniques. However, the pure p-well isolation was achieved with high spacing leading to low fill factor (FF) and the hybrid-p-well isolation was compared to the STI isolation by keeping a similar FF. In fact, most of these techniques can lead to reduction of the FF and, hence, of the optical performance. Nevertheless, they are an effective way to reduce the DC from a design perspective.

In this paper, we propose a layout sharing technique for 4 transistors (4T) CMOS pixels which optimises the isolation mechanism to reduce the DC. We use a hybrid scheme, where the pixels are folded consenting to remove the STI between adjacent PDs, while remaining it between the PDs and the in-pixel-transistors. This technique has been evaluated on CIS test-chips manufactured in a commercially available image sensors process technology: the enhancement of the full-well capacity (FW) and the decrease of the DC for same-pitch pixels has been demonstrated experimentally.

The paper is organised as follows: Section II describes the pixel design with focus on the isolation scheme. Section III provides the characterisation results based on the pixel parameters of the manufactured samples. Finally, in Section IV the conclusions of the paper are drawn.

II. Pixel Design

We have designed a CIS based on a 4T pixel unity cell. The design strategy was aimed at reducing the DC component due to the isolation mechanism.

Fig.1a shows the 4T pixel schematic, including: the *PD*, which is a pinned photodiode accessed through the transfer

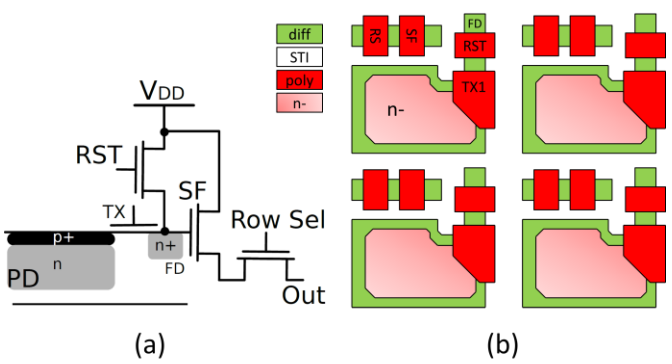

Fig. 1. (a) Schematic of a 4T Pixel and (b) layout of a typical 2-by-2 4T pixel block in CMOS technology.

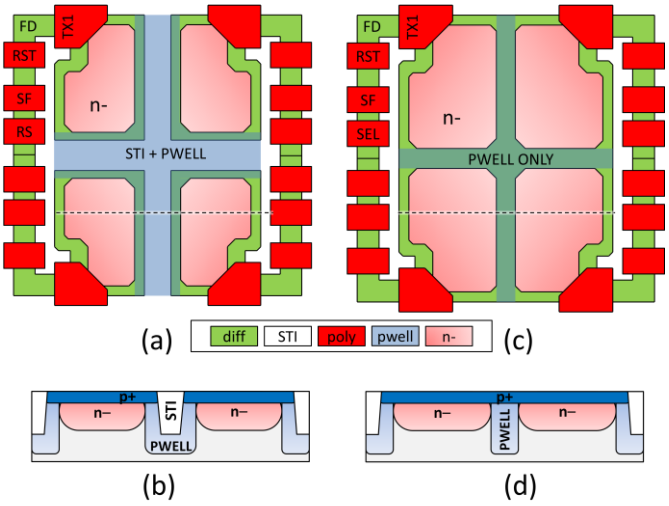

Fig. 2. Sketches of the top-view layouts and of the related cross sections of four 4T-pixel blocks with STI (a and b, respectively) and hybrid isolation (c and d, respectively).

gate *TX*; *RST* is the reset transistor while *SF* and *Row-Sel* are the source follower and the row selector transistors, respectively. In the pixel array, *TX*, *RST* and *Row-Sel* are row control signals, while the supply voltage V_{DD} and *Out* are shared among pixels in the same column. Fig.1b shows a possible conventional layout implementation of a 2-by-2 block of 4T pixels. The STI is represented by the white background surrounding all active areas, including the transistors and the PD. It is possible to rearrange this layout by placing the two edges of adjacent PDs to have one facing another as shown in Fig.2a. This configuration still uses STI to isolate the PDs and will be referred to as STI-pixel. In addition, this arrangement leads to improvement in drawing global wires (not shown) and can lead to enhancement of the overall FF. It is worth noting that this approach leads to a loss of the translational symmetry required for conventional microlenses. Nevertheless, one can use a dual microlens process with different focusing directions. Furthermore, the symmetry is preserved at the block level of 2x2 pixels without impacting Fixed-Pattern Noise (FPN) between color planes. The related vertical cross-section highlighting the isolation between two neighbouring PDs is shown in Fig.2b.

STI, though reliable and commonly used, is not the only mechanism available to provide isolation between active layers in a CMOS process. For example, two n-type diffusions can be separated by a p-type implantation as long as it does not lead to a forward biased diode or to a punch-through in the resulting n-p-n parasitic transistor. A simple p-type diffusion available to all designers is the p-well. As shown in Fig.2c and d, this consumes significantly less area than the STI on the silicon surface. Removing the STI in the central region between the active n-diffusions allows to shrink the required spacing between two PDs. This means that the area gained by using a p-well (in place of common STI/p-well) can be used to further enlarge the PD, thereby increasing the pixel FW.

Previous approaches reported in literature have aimed to entirely remove the STI by surrounding the photodiode with a different layer (p-well or polysilicon guard ring) [11]. However, it is worth recalling that in a standard pixel, the STI surrounds the entire PD as it is needed for electrical isolation especially close to the transistors. Unfortunately, the p-well layer provides less isolation compared to the STI. Hence, it cannot be exploited to isolate the in-pixel transistors unless a very large distance is used, with clear reduction of the FF. Hence, a complete removal of the STI is likely to be counterproductive.

The hybrid approach we propose is to use conventional STI between the PD and the transistors, while p-well only is used between neighbouring PDs. Fig.2c and d show this hybrid pixel design approach (layout top view and cross-section, respectively), which will be referred to as hybrid-isolation-pixel. The STI has been removed between the diodes, with isolation granted by a p-well, while the STI is still used for separating the PDs with active transistors. Such a technique was expected to provide the required isolation as well as an increase in the FF, while reducing the DC, without impacting the electron collection efficiency. To test this design, several chips were fabricated in LFoundry 110 nm CMOS image sensor process technology. The pixel pitch of the manufactured pixels is 2.4 µm. Both types of pixels with their isolation mechanisms, STI and hybrid-isolation, were manufactured in different test circuits fabricated on the same wafer.

III. Pixel Characterisation

The photoresponse curves of the samples manufactured with the two different layouts reported in Fig.3 were measured as follows. A constant light source with a green LED centred at a wavelength of 550 nm and with a power of 1.97 µW/m^2 was used for these experiments. Both the signal and the temporal noise were evaluated from a set of images for each data point on a window of 186-by-84 pixels to extract the photon transfer curve (PTC), which has been measured according to the EMVA1288 standard [24]. Fig.3 shows the PTC for the tested STI-pixel and the hybrid-isolation-pixel versions. The figure shows similar behaviour between the two

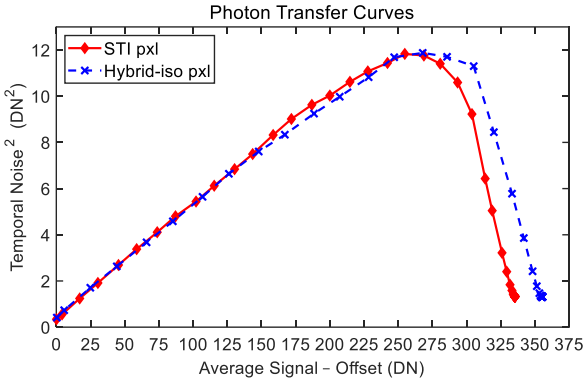

Fig. 3. Measured Photon Transfer Curve for the STI-pixel and hybrid-isolation-pixel.

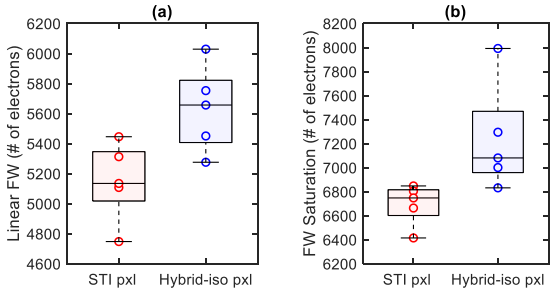

Fig. 4. Statistical variation of the (a) linear-full-well and (b) full-well-saturation expressed in electrons as measured from the STI-pixel and hybrid-isolation-pixel.

pixels. At high signal levels, the hybrid layout leads to improved performance due to its differences in full well capacity, despite similar conversion factor, FPN and read noise between the pixels. In this study, a set of close dice within the same wafer was analysed to highlight layout-related effect on the Full Well, while minimising the impact of process-related variations.

Fig.4 (a) and (b) show the measured values (averaged on the whole pixel array) of the linear full well (LFW) and of the full well saturation level, respectively. Note that the hybrid-isolation-pixel has higher full-well capacity than its STI-pixel counterpart. Linear and saturation FW are approximately 480 and 540 electrons higher in case of the hybrid-isolation-pixel.

Table I compares the extracted linear and saturation FW of the presented curves to their respective fill factor, photodiode area and perimeter. The increase in FF is correlated to the full well capacity values. This is coherent with the expectation of an increase in the saturation value for a photodiode with a larger active area. Note that the increase in saturation level did not scale linearly with the FF. An increase of the FF of 24% only gives an enhancement in linear full well and saturation levels of 9.3% and 8.1%, respectively. One possible explanation for this limit could be the non-rectangular shape of the photodiode, which was used to maximise its area.

The impact of STI-removal towards the dark current reduction was evaluated next. Similarly to the EMVA1288 Standard [24], the DC is measured by capturing multiple (40) dark images with six equally-spaced increasing integration

TABLE I
COMPARISON BETWEEN THE PROPOSED PIXEL LAYOUTS

Parameter	STI-pixel	Hybrid-isolation-pixel	Improvement [%]
Linear full-well [e]	$5.15{\cdot}10^3$	$5.63{\cdot}10^3$	9.3
Saturation level [e]	$6.69{\cdot}10^3$	$7.24{\cdot}10^3$	8.1
PD perimeter [µm]	5.63	5.88	4.4
PD area [µm^2]	1.69	2.08	23
Fill Factor [%]	29	36	24
Dark current [e/s]	133	105	-21

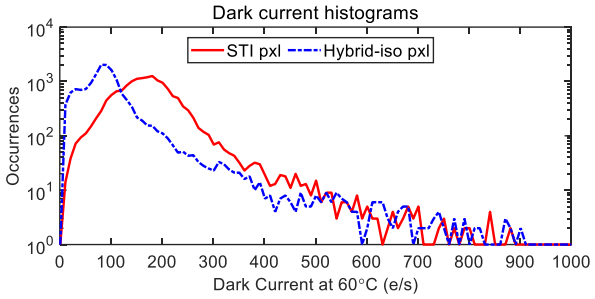

Fig. 5. Dark current distributions as measured on one representative sample for each test-array (186-by-84 pixels) of the STI-pixel and hybrid-isolation-pixel.

times. Fig.5 illustrates the typical DC distribution of the pixel array measured at 60 °C on one representative sample for each design variation. The interesting features in these histograms are the principal peak (i.e., the mode of the distribution) and the tail of the dark current profiles. The histograms are plotted on semilogarithmic y-axis for better appreciation of these features. It is evident that both peak and shoulder of the distribution are located at lower DC values for the hybrid scheme compared to the STI-pixel, while the tail is similar. These measurements indicate that the avoidance of STI/active-area edges in the hybrid-isolated pixel decreases the number of interface defects, thereby reducing the dark current.

It is worth noting that a photodiode area increase may intrinsically lead to higher dark current due to larger number of thermally generated charge carriers [25]. The lower dark current obtained for a larger fill-factor pixel further confirms the effectiveness of our results. Table I shows the percentage difference between the average dark current of the STI-pixel and the hybrid-isolation-pixel. The net decrease in dark current is 21% despite an increase in photodiode area and perimeter of 23% and 4.4% respectively. If the increase in photodiode area is taken into account (by normalisation), the actual estimated dark current reduction for two pixels having the same photodiode area would be of approximately 26%.

In conclusion, we have demonstrated that a folded pixel design with the STI around the transistors and the p-well between the pixel active areas, significantly improves the pixel performance. In particular, the hybrid approach results in lower dark current, higher full-well capacitance, and higher fill factor than the STI-only approach, while preserving a good isolation of the transistors.

IV. Conclusions

In this paper, a folded pixel design which enables a hybrid p-well/STI isolation scheme is proposed to reduce the dark current while increasing the full well capacity and fill factor of the pixels. This layout design has been applied to 4T CMOS pixels, removing the STI between neighbour photodiodes and only remaining the p-well. The STI was maintained between the transistors to ensure good isolation between the devices. This idea has been verified by comparing the proposed Hybrid-isolated proposal to a reference STI layout implemented and manufactured in a commercial image sensor process. Measurements on the final test chips have shown that the hybrid-isolation-pixel is able to increase the linear full well of the photodiodes of approximately 9% while reducing the dark current by 21% compared to the STI-pixel. These remarkable performance improvements have been achieved just by optimising the design, without any costly process modification. The proposed approach can be easily applied to any other process technology and to other pixel architectures. In conclusion, this is a valuable approach demonstrating a simple layout rearrangement to achieve higher fill-factor, higher full-well capacity, and lower dark current compared to standard pixels. This is the recommended option to get the best tradeoff among low leakage and good fill factor.

Acknowledgment

The authors thank Andrea Del Monte, Giuseppe Di Nicolantonio, and Giovanni De Amicis for their many helpful discussions on the process technology and characterisation techniques. The authors also thank Martin Wäny for the constructive comments, help and support to design the test chips. They also acknowledge LFoundry for the fabrication of the prototype image-sensors.

References

[1] E. R. Fossum and D. B. Hondongwa, "A Review of the Pinned Photodiode for CCD and CMOS Image Sensors," in IEEE Journal of the Electron Devices Society, vol. 2, no. 3, pp. 33-43, May 2014. DOI: 10.1109/JEDS.2014.2306412

[2] O. Marcelot, V. Goiffon, F. Nallet and P. Magnan, "Pinned Photodiode CMOS Image Sensor TCAD Simulation: In-Depth Analysis of in-Pixel Pinning Voltage Measurement for a Diagnostic Tool," in IEEE Transactions on Electron Devices, vol. 64, no. 2, pp. 455-462, Feb. 2017. DOI: 10.1109/TED.2016.2634601

[3] V. Goiffon et al., "Pixel Level Characterization of Pinned Photodiode and Transfer Gate Physical Parameters in CMOS Image Sensors," in IEEE Journal of the Electron Devices Society, vol. 2, no. 4, pp. 65-76, July 2014. DOI: 10.1109/JEDS.2014.2326299

[4] S. Rizzolo, V. Goiffon, M. Estribeau, O. Marcelot, P. Martin-Gonthier and P. Magnan, "Influence of Pixel Design on Charge Transfer Performances in CMOS Image Sensors," in IEEE Transactions on Electron Devices, vol. 65, no. 3, pp. 1048-1055, March 2018. DOI: 10.1109/TED.2018.2790443

[5] R. Capoccia, A. Boukhayma, F. Jazaeri and C. Enz, "Compact Modeling of Charge Transfer in Pinned Photodiodes for CMOS Image Sensors," in IEEE Transactions on Electron Devices, vol. 66, no. 1, pp. 160-168, Jan. 2019.DOI: 10.1109/TED.2018.2875946

[6] Hsiu-Yu Cheng and Ya-Chin King, "An ultra-low dark current CMOS image sensor cell using n/sup +/ ring reset," in IEEE Electron Device Letters, vol. 23, no. 9, pp. 538-540, Sept. 2002. DOI: 10.1109/LED.2002.802587

[7] Hyuck In Kwon, In Man Kang, Byung-Gook Park, Jong Duk Lee and Sang Sik Park, "The analysis of dark signals in the CMOS APS imagers from the characterization of test structures," in IEEE Transactions on Electron Devices, vol. 51, no. 2, pp. 178-184, Feb. 2004. DOI: 10.1109/TED.2003.821765

[8] C. Moon, J. Jung, D. Kwon, J. Yoo, D. Lee and K. Kim, "Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors," in IEEE Electron Device Letters, vol. 28, no. 2, pp. 114-116, Feb. 2007. DOI: 10.1109/LED.2006.889241

[9] J. Carrère, S. Place, J. Oddou, D. Benoit and F. Roy, "CMOS image sensor: Process impact on dark current," 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, 2014, pp. 3C.1.1-3C.1.6. DOI: 10.1109/IRPS.2014.6860620

[10] M. Seo, S. Kawahito, K. Yasutomi, K. Kagawa and N. Teranishi, "A Low Dark Leakage Current High-Sensitivity CMOS Image Sensor With STI-Less Shared Pixel Design," in IEEE Transactions on Electron Devices, vol. 61, no. 6, pp. 2093-2097, June 2014. DOI: 10.1109/TED.2014.2318522

[11] B. Choubey and S. Collins, "Wide dynamic range CMOS pixels with reduced dark current," Analog Integrated Circuits and Signal Processing, vol. 56, no. 1-2, pp. 53–60, 2008.

[12] A. W. Ballantine, G. A. Dunbar III, J. V. Hart III, D. K. Johnson, and G. C. MacDougall, "Method for reducing dark current effects in a charge couple device," Aug. 7 2001. US Patent 6,271,054.

[13] M. Lee, S. Barabash, T. Chiang, and D. Pramanik, "Fluorine passivation in CMOS image sensors," Sept. 18 2014. US Patent App. 14/137,866.

[14] J. Janesick, "CMOS multi-pinned (mp) pixel," Sept. 23 2015. EP Patent App. EP20,130,855,265.

[15] J. Hynecek and H. Komori, "CMOS image sensor having global shutter pixels built using a buried channel transfer gate with a surface channel dark current drain," June 25 2013. US Patent 8,471,315.

[16] R. Hsiao, N. Cheng, C. Lin, C. Tseng, and S. Wuu, "Stress engineering to reduce dark current of CMOS image sensors," Oct. 1 2013. US Patent 8,546,860.

[17] B. Mheen, Y. Song and A. J. P. Theuwissen, "Negative Offset Operation of Four-Transistor CMOS Image Pixels for Increased Well Capacity and Suppressed Dark Current," in IEEE Electron Device Letters, vol. 29, no. 4, pp. 347-349, April 2008. DOI: 10.1109/LED.2008.917812

[18] S. Manabe and J. Lyu, "Ground contact structure for a low dark current CMOS pixel cell," Feb. 26 2014. EP Patent App. EP20,130,172,885.

[19] S. Takahashi, Y.-M. Huang, J.-J. Sze, T.-T. Wu, F.-S. Guo, W.-C. Hsu, T.-H. Tseng, C.-C. Liao, C.-C. Kuo, T.-H. Chen, W.-C. Chiang, C.-H. Chuang, K.-Y. Chou, C.-H. Chung, K.-Y. Chou, C.-H. Tseng, C.-J. Wang, and D.-N. Yaung, "Low Dark Current and Low Noise 0.9 μm Pixel in a 45 nm Stacked CMOS Image Sensor Process Technology," Proceedings of the International Image Sensors Workshop, 2017.

[20] A. M. Brunetti and B. Choubey, "A low dark current wide dynamic range CMOS pixel," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 2523-2526. DOI: 10.1109/ISCAS.2016.7539106

[21] S. W. Han and E. Yoon, "Low dark current CMOS image sensor pixel with photodiode structure enclosed by P-well," in Electronics Letters, vol. 42, no. 20, pp. 1145-1146, 28 September 2006. DOI: 10.1049/el:20061652

[22] B. Choubey and S. Collins, "Low dark current logarithmic pixels," 48th Midwest Symposium on Circuits and Systems, 2005., Covington, KY, 2005, pp. 376-379 Vol. 1. DOI: 10.1109/MWSCAS.2005.1594116

[23] S. H. Choi, Y. T. Kim, M. S. Oh, Y. H. Park, J. J. Cho, Y. H. Jang, H. J. Han, J. W. Choi, H. W. Park, S. I. Jung, H. S. Oh, J. C. Ahn, H. Goto, C. Y. Choi, and Y. Roh, "A novel pixel design with hybrid type isolation scheme for low dark current in CMOS image sensor," in Proc. SPIE, vol. 8659, pp. 86590F–86590F–8, 2013

[24] Bernd Jähne, "EMVA 1288 Standard for Machine Vision", in Optik & Photonik, vol. 5 n.1, pp. 53-54, 2010. DOI: 10.1002/opph.201190082

[25] N. V. Loukianova et al., "Leakage current modeling of test structures for characterization of dark current in CMOS image sensors," in IEEE Transactions on Electron Devices, vol. 50, no. 1, pp. 77-83, Jan. 2003. DOI: 10.1109/TED.2002.807249