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Low Frequency Noise and Gate Bias Instability in Normally-Off AlGaN/GaN HEMTs

Felice Crupi, *Senior Member, IEEE*, Paolo Magnone, Sebastiano Strangio, Ferdinando Iucolano, Gaudenzio Meneghesso, *Fellow IEEE*

***Abstract* — In this paper, traps-related dispersion phenomena are investigated on GaN/AlGaN MOS-HEMTs. Pulsed I-V characteristics and low-frequency-noise measurements are the characterization vehicles used to get a direct insight of the device trap-states. By considering a set of 10 samples, device-to-device fluctuation parameters extracted from trap-related measurements (1/f noise and gate bias instability) are systematically compared with conventional electrical parameters (threshold voltage and on-current). Two separate trends are identified and ascribed to two different trap families.**

***Index Terms*— GaN, MOS-HEMT, traps, low frequency noise, gate bias instability, threshold voltage.**

I. Introduction

THE requirements of higher efficiency and higher power density in power electronics calls for performant switching devices, exhibiting low conduction losses and high operating frequency. In this field, GaN High Electron Mobility Transistor (HEMT) represents a valuable solution, because of the improved breakdown voltage/on-resistance trade-off, higher temperature capability and larger operating frequency, with respect to conventional Si-based devices. An important limitation of GaN devices is represented by current collapse phenomenon, leading to an increase of dynamic resistance when operating in switching conditions [1-4]. Recent studies [5-7] have demonstrated that traps responsible for current collapse are localized in the buffer layer. On the other hand, normally-off transistors are required for circuital applications, hence avoiding the adoption of complicated drive solutions (e.g. cascade solutions for the control of normally-on devices).

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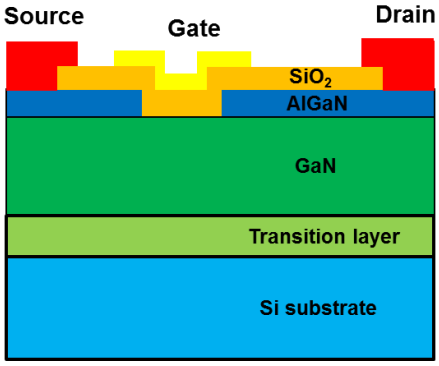

Fig. 1. Sketchof the AlGaN/GaN MOS-HEMT under investigation.

Among the different approaches to achieve normally-off devices, GaN-based hybrid MOS-HEMTs have been proposed [8]. In the case of MOS-HEMT or MIS-HEMT architectures, threshold voltage instability under gate bias stress have been proved to limit on- current and resistance [9-11].

Given the importance of trap distribution in GaN HEMTs, low-frequency noise (LFN) measurements represent a powerful tool for the analysis of these devices. This technique has been widely applied to the field of CMOS technology, in order to assess the defectiveness of materials and in particular of gate dielectric [12-15]. Recently, the validity of LFN measurements has been proved in the case of power semiconductor devices, such as power MOSFETs [16] or GaN HEMTs [17, 18].

In this paper, a study of LFN is performed on AlGaN/GaN MOS-HEMTs, aiming at understanding the distribution of defects in the structure. By conducting a correlation analysis among LFN, gate bias instability and conventional electrical parameters (threshold voltage and on-current), we are able to identify two types of defect.

II. Experimental

HEMTs have been fabricated on AlGaN/GaN heterostructures grown on Si (111) substrates. The recessed approach has been used to obtain a normally-off device. A schematic cross section of the fabricated recessed hybrid MOS-HEMT structure is reported in Fig. 1. The ohmic contacts were formed by Ti/Al-based metallization, while Ni-based were used for the gate contact. Details on the ohmic and gate contacts formation can be found in [19] and [20],

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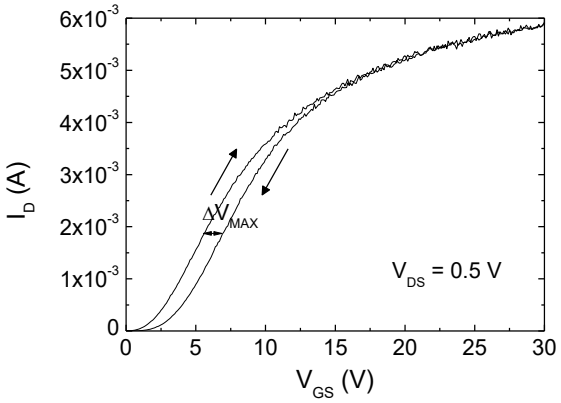

Fig. 2. Drain current as function of pulsed gate voltage. The hysteresis observed in the I-V curve is quantified by evaluating the maximum gate voltage shift ΔV_{MAX} for different I_D values.

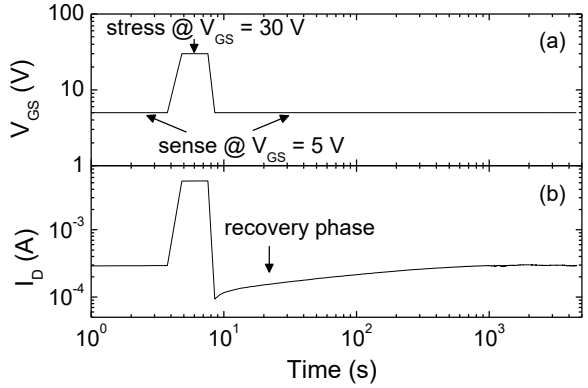

Fig. 3. Drain current dynamics after applying a positive voltage stress. The device exhibits a recovery time in the order of minutes.

respectively. The AlGaN layer was recessed using a dry etch process in a chlorine-based chemistry. As gate insulator, SiO_2 layer (50 nm thick) was deposited by plasma enhanced chemical vapour deposition using tetraethyl orthosilicate (TEOS) precursor, and subjected to a thermal annealing at 850°C in N_2.

We used two different types of electrical characterization techniques, LFN and pulsed I-V. LFN measurements were performed by using a purposely designed measurement system, consisting of two low noise bias stages (for the gate and the drain terminal) and a low noise trans-impedance amplifier [14, 16]. Noise data were acquired by biasing the devices in linear regime with V_{DS} = 500 mV. Pulsed I-V measurements were carried out by means of a parameter analyzer Keithley 4200-SCS equipped with the 4225-PMU ultra fast I-V module and two 4225-RPM remote amplifier/switch modules. I-V curves were obtained by applying a train of pulses with a period of 300 µs and a width of 30 µs at the gate and drain terminals. The gate voltage pulse amplitude was varied from 0 to 30 V with a step of 100 mV, while the drain voltage pulse amplitude was kept constant at 500 mV. Overall, the time required to sweep V_{GS} from 0 V up to 30 V is 90 ms, while the effective stress time is 9 ms. In order to perform a correlation analysis on different device electrical parameters, experiments are carried out on a set of 10 samples.

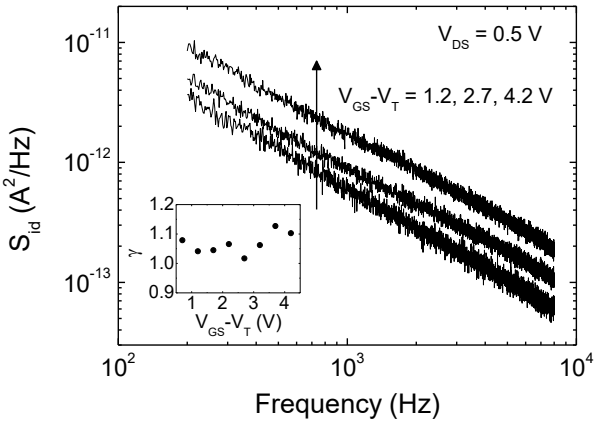

Fig. 4. Power spectral density of the drain current noise. Typical flicker $1/f^{\gamma}$ noise is observed. As reported in the inset, γ values are very close to 1.

III. Results and Discussion

A typical pulsed I_D-V_{GS} curve of a normally-off GaN HEMT is reported in Fig. 2. Even if the pulse time is reduced down to 30µs, a significant hysteresis is observed on the I-V curve when sweeping V_{GS} from 0 V up to 30 V and then down to 0 V again. As observed in [9-11], the reduction of current can be ascribed to traps located at the oxide/GaN interface or in the lateral regions, leading to a change of the threshold voltage. In order to quantify the hysteresis in the I-V curve, we measured the maximum voltage shift ΔV_{MAX} as reported in Fig. 2. The dynamics of drain current, following a gate voltage stress (30 V for xx s), is reported in Fig. 3. The recovery phase, required in order to bring the drain current level back to the initial value, is in the order of minutes. Hence, traps involved during forward bias stress show a highly asymmetric trapping and detrapping time.

The power spectral density (PSD) of the drain current is reported in Fig. 4 for different gate voltage overdrive (V_{GS}-V_{Th}). It is worth noting that noise measurements were carried out in fresh devices under stationary conditions. As shown in the inset, $1/f^{\gamma}$ noise, with γ very close to 1, is observed for all the considered bias conditions. The normalized drain current spectra are then plotted against the gate voltage overdrive in Fig. 5a. Experimental data are fitted with the function $S_{ID}/I_D^2 \propto |V_{GS}-V_T|^{\alpha}$. The slope α of this plot gives information about the fundamental fluctuation mechanism [14]. In particular, being the slope close to −1, mobility fluctuation can be assumed as the source of fluctuation for the drain current. In this case, it is well known that defects responsible for the1/f noise are physically located in the gate dielectric. Moreover, 1/f noise arising from source and drain series- resistance can be assumed negligible, since a normalized noise independent of the bias point would be expected for this case [21]. As a result we can assert that 1/f noise is mainly related to traps located in the gate region. In particular, both gate dielectric quality and SiO_2/GaN interfacial defects (due to plasma deposition) could be responsible for the 1/f noise.

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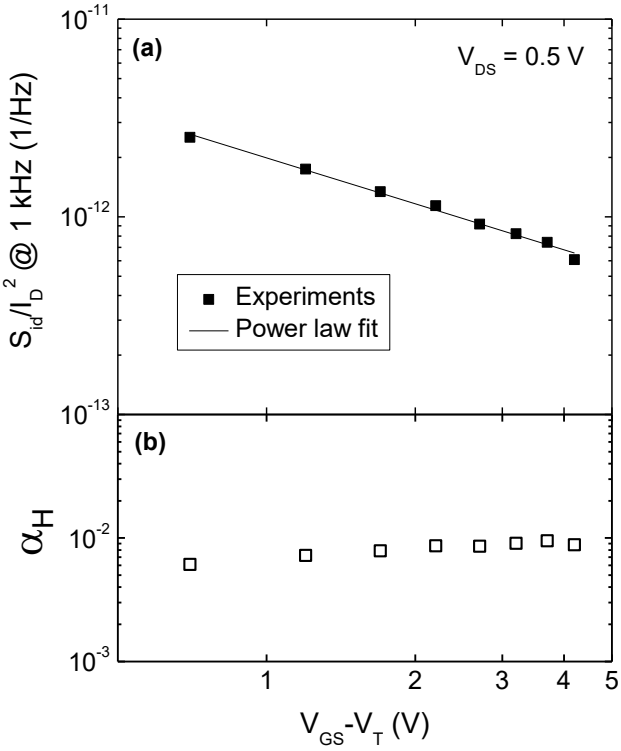

Fig. 5. (a) Normalized S_{id} as a function of gate voltage overdrive. Being the slope α close to -1 (and in particular equal to -0.8), mobility fluctuation can be assumed as the source of flicker noise. (b) Hooge parameter (α_H) calculated according to the mobility fluctuation model [14]. The Hooge parameter is larger than what typically observed in silicon-based MOS devices (10^{-3}).

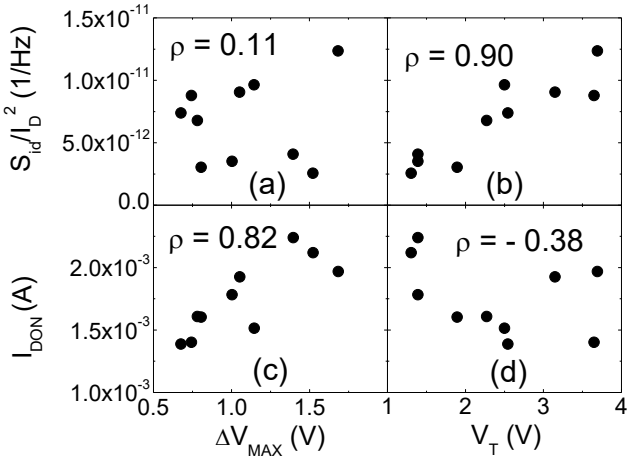

Fig. 6. Correlation plots: S_{id}/I_D^2 vs. ΔV_{MAX} (a), S_{id}/I_D^2 vs. V_T (b), I_{DON} vs. ΔV_{MAX} (c) and I_{DON} vs. V_T (d). Strong correlation is observed between the drain current noise and threshold voltage (b) and between gate voltage shift and on-current (c).

According to the mobility fluctuation model, the so-called Hooge parameter can be estimated [14], representing a figure of merit of the MOS quality. In Fig. 5b we can observe that, the value obtained for AlGaN/GaN MOS-HEMTs is significantly larger than what typically found in MOSFET devices (in the order of 10^{-3}) [14], pointing out a relevant defectiveness of SiO_2/GaN interface.

In Fig. 6 we report correlation plots among the following parameters: i) normalized flicker noise S_{ID}/I_D^2 at f = 1kHz and I_D = 300 μA; ii) gate voltage shift ΔV_{MAX} due threshold voltage instability; iii) threshold voltage V_T in fresh devices; iv) drain current I_{DON} at fixed gate voltage overdrive (V_{GS} - V_T = 5V) in fresh devices. As shown in Fig. 6a, S_{ID}/I_D^2 and ΔV_{MAX} are basically uncorrelated parameters. This means that 1/f drain current fluctuations and gate bias instability phenomenon origin from different defects. Since LFN measurements are performed at low gate voltage, we can assume negligible degradation occurs in the device. Therefore, noise is mainly related to defects in the fresh device. On the other hand, when considering a large gate bias stress (as in the case of ΔV_{MAX} measurement), a significant number of charges can be trapped close to the SiO_2/GaN interface. The experimental uncorrelation points out that the amount of V_T instability is not related to the initial LFN and to traps affecting the transport at low gate voltage. Different scenarios are then possible for the traps involved during gate bias stress: i) could be those in the lateral regions (as suggested in [10]); ii) could be those under the gate region but having different energy with respect to those involved in LFN analysis; iii) new defects could be generated during the stress. Considering the complete recovery observed in Fig. 3, the hypothesis of generation of new defects is hardly plausible.

Given the amount of cumulative stress time received by the samples (18 ms during the sweep in both directions), the measured ΔV_{MAX} (in the order of 1V) is significantly large. In fact, Guo et al. [9] reported that in a MOS-HEMT with 50nm of SiO_2 oxide, a gate voltage stress of 15V must be applied for about 10^4 s in order to obtain a comparable degradation. Moreover, as opposite to our case, a significant permanent degradation was observed.

As reported in Fig. 6b, 1/f noise is strongly correlated with the device threshold voltage. Therefore, the significant threshold voltage variability can be ascribed to the defects in gate dielectric or at the SiO_2/GaN interface, affecting the work-function of the MOS structure. In Fig. 6c, a strong correlation between ΔV_{MAX} and I_{DON} is observed, meaning that devices exhibiting larger drain current are subject to a larger threshold voltage instability. Moreover, according to Fig. 6d, the variation of on-current cannot be ascribed to the initial threshold voltage, since a weak correlation is observed.

IV. Conclusions

In this paper, we analyzed 1/f drain current noise along with threshold voltage instability effects in AlGaN/GaN MOS-HEMTs. The low frequency noise analysis pointed outa 1/f trend on mobility fluctuation basis, characterized by a Hooge parameter close to 10^{-2}. This relatively large value can be ascribed to the defectiveness of SiO_2/GaN interface. These defects are also responsible for therelevant dispersion of the threshold voltage in fresh devices. On the other hand, the correlation analysis highlighted that threshold voltage instability seems to be related to different defects, perhaps having different energy or localized in the lateral regions.

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Furthermore, samples exhibiting a larger threshold voltage instability also show a larger on-current, even if the current level is uncorrelated with the initial threshold voltage.

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