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Waveguide-integrated, plasmonic enhanced graphene photodetectors

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We present a micrometer scale, on-chip integrated, plasmonic enhanced graphene photodetector (GPD) for telecom wavelengths operating at zero dark current. The GPD is designed and optimized to directly generate a photovoltage and has an external responsivity∼12.2V/W with a 3dB bandwidth∼42GHz. We utilize Au split-gates with a∼100nm gap to electrostatically create a p-n-junction and simultaneously guide a surface plasmon polariton gap-mode. This increases light-graphene interaction and optical absorption and results in an increased electronic temperature and steeper temperature gradient across the GPD channel. This paves the way to compact, on-chip integrated, power-efficient graphene based photodetectors for receivers in tele and datacom modules.

The ever-growing demand for global data traffic[1] is driving the development of next generation communication standards[2, 3]. The increasing numbers of connected devices[4], the need for new functionalities, and the development of high-performance computing[5, 6] require optical communication systems performing at higher speeds, with improved energy-efficiency, whilst maintaining scalability and cost-effective manufacturing. Si photonics[7–9] offers the prospect of dense (nanoscale) integration[10] relying on mature, low-cost (based on complementary metal-oxide-semiconductor (CMOS) fabrication processes) manufacturing[8, 9], making it one of the key technologies for short-reach (<10km) optical interconnects[11] beyond currently employed lithium niobate[12] and indium phosphate[13].

A variety of functionalities have been developed and demonstrated in Si photonics for local optical interconnects[11]. Electro-optic modulators based on carrier-depletion (phase-modulation) in Si[14, 15] or the Franz-Keldysh effect[16] (amplitude-modulation) in strained Si-Ge[17, 18] encode information into optical signals at telecom wavelengths (λ =1.3-1.6μm). On the receiver side, Ge[19] or bonded III-V[20, 21] photodetectors (PD) are needed for optical-to-electrical signal conversion, since the telecom photon energies are not sufficient for direct (band-to-band) photodetection in Si[22].

On-chip integrated Ge PDs[23–27] are standard components in Si photonics foundries[8, 9, 22]. Their external responsivities (in A/W), $R_I = I_{\rm ph}/P_{\rm in}$, where $I_{\rm ph}$ is the photocurrent and $P_{\rm in}$ is the incident optical power, can exceed 1A/W[8, 23] and their bandwidth can reach 60GHz[25–27]. Following the development of high temperature ($> 600°$C)[19] heterogeneous integration of Ge-on-Si using epitaxial growth and cyclic thermal annealing[19, 28, 29], the concentration of defects and threading dislocations in Ge epilayers and at Si/Ge interfaces can be reduced[19], resulting in low (<10nA[9, 27]) dark current in waveguide integrated Ge p-i-n photodiodes[24, 27]. However, Ge-on-Si integration is a complex process[19, 22, 29], as the lattice mismatch between Si and Ge[19], ion implantation[23, 25], thermal budget (i.e. thermal energy transfer to the wafer) management[22], and the non-planarity of Ge layers[29] require dedicated solutions during device fabrication[9]. The charge carrier mobility μ in Si and the dislocations and defects in grown[19] or evaporated[30] Ge layers set intrinsic limitations that prevent further improvements to the operation speed of Ge PDs without compromising R_I[9, 26]. These shortcomings, together with the spectrally limited operation regime (band edge in Ge$\sim 1.57\mu$m[22], which can be extended to$\sim 1.62\mu$m[31] at the expense of R_I), and the incompatibility of Ge epitaxy for monolithic integration with other material platforms, such as SiN, are amongst the main limitations for Ge PDs[8]. Thus, novel solutions for PDs, integrated with Si photonics, at telecom bands are needed.

Graphene is a promising candidate for on-chip integrated photonics[32–52]. The advantages of single-layer graphene (SLG) for photonics stem from its superior optoelectronic properties[53]. These include high-speed (>200GHz[54]) operation[55], broadband (ultraviolet to far-infrared) absorption[56–58], efficient optical modulation (electro-optical index change $\Delta n_{\rm eff} > 10^{-3}$)[32–38], CMOS compatibility[41, 59] and integrability[32, 60, 61] with different on-chip photonics platforms, such as silicon-on-insulator (SOI)[33] and SiN[36]. In the case of waveguide-integrated graphene PDs (GPDs)[40–52], high speeds up to 128GHz[49], wafer-scale integration[48]

and R_I ~0.4-0.5A/W[43, 47, 50, 51] were reported. GPDs can offer broadband detection across multiple telecommunication channels (O-band~1.31μm to U-band~1.65μm)[41], bias-free operation[62], and direct generation of photovoltage[45, 62]. The latter opens up the possibility of building GPDs without the noise contribution of dark current[32, 46] and eliminates the need of noise-prone trans-impedance amplifier (TIA) to convert current-to-voltage in the read-out electronics[32].

GPDs can be built exploiting different mechanisms: photo-voltaic (PV)[55, 63, 64], photo-thermoelectric (PTE)[64–66], photo-gating[67], plasma-wave assisted[68] and photo-bolometric (PB)[69, 70]. The dominating effect for a given GPD depends on device configuration, design geometry, and way of operation[64, 71]. For telecom applications, where high-speed (tens GHz) operation is one of the key requirements[8, 32], PV, PTE and PB are typically considered for waveguide-integrated GPDs[32], taking advantage of the ultra-fast (~fs-ps) carrier dynamics in SLG[72, 73].

PTE is ideal for PD operation in a voltage mode. In optically illuminated SLG, electron-electron scattering drives the formation of a 'hot' (optically excited)-carrier distribution, described by the Fermi-Dirac function[74], within <50fs[72]. This can remain at elevated temperatures T_e, well above the lattice temperature T_l, over~2-4ps time scales[72], before reaching thermal equilibrium via phonons interaction[73, 75, 76]. In this hyperthermal state, a photovoltage $V_{\rm ph}$ is generated by a thermoelectric current as for the Seebeck effect[66], if both a temperature and chemical potential gradient are present in the SLG channel. The sign and magnitude of $V_{\rm ph}$ depend on the Seebeck coefficient (S), i.e. the proportionality constant between temperature change and induced photovoltage[77], and $T_{\rm e}$ profile in the SLG channel[66]:

$$V_{\rm ph} = \int S(x) \cdot \nabla T_e(x)\, {\rm d}x \qquad (1)$$

where x is the coordinate along the channel from drain to source, and S is given by Mott's formula[64–66, 77]:

$$S(x) = -\frac{\pi^2 k_{\rm B}^2 T_e}{3e} \frac{1}{\sigma(x)} \frac{{\rm d}\sigma(x)}{{\rm d}\mu_c} \qquad (2)$$

with $\sigma(x)$ the conductivity, $k_{\rm B}$ the Boltzmann constant, e the electron charge and μ_c the chemical potential ($\mu_c = E_F$ at $T_e = 0$[74], with E_F the Fermi energy).

PTE-GPDs have been reported in vertically-illuminated[66, 78–81] and waveguide-integrated[45–47]configurations. The latter used SLG flakes prepared by micromechanical cleavage (MC) of graphite[82], with typical device length of tens of μm[45–47]. They have external voltage responsivities, defined as $R_V = V_{\rm ph}/P_{\rm in}$, up to~4.7V/W[46] (at zero bias) with speeds up to 65GHz[45]. Depending on PTE-GPD design configuration and the requirements of the read-out electronics (i.e. output photo-signal to be measured as current or voltage), the responsivity can be characterized in terms of R_I or R_V. The photovoltage generated by the Seebeck effect is associated with a thermoelectric current across the PD by a Ohmic relation[45, 46, 62, 79] $I_{\rm ph} = V_{\rm ph}/R$, with R the resistance.

To increase R_V for PTE-GPDs, Eq.1 suggests two strategies: 1) maximize S; 2) maximize the $T_{\rm e}$ gradient profile in the SLG channel. The former is related to μ via Eq.2 and the Drude conductivity[77], $\sigma = e\mu n$, where n is the charge carrier concentration. Thus, S can be improved by using high-mobility SLG, e.g. encapsulating SLG in hBN[83–85], using single-crystals[85, 86], or large (tens μm) domain-size[87], in combination with a transfer processes that avoid contamination[84, 88], strain[88], and cracks[89]. Ref.[32] suggested that $\mu > 10^4{\rm cm}^2{\rm V}^{-1}{\rm s}^{-1}$ could enable $R_V >$ 100V/W. The T_e gradient can be increased by creating a spatially confined, localized, heat source[45] generated by enhanced optical absorption in SLG over compact ($< 10\mu$m) device lengths[50, 51]. This could be achieved by integrating plasmonic nanostructures[90–95]. Sub-wavelength plasmonic confinement and associated enhancement of near-field light-matter interaction were used to boost R_I in Si-plasmonic PDs[90, 91], plasmonic-Ge PDs[92], plasmonic decorated GPDs for free-space[93–95] and waveguide-integrated[43, 50–52, 96] configurations. Refs.[50–52] reported plasmonic enhanced on-chip GPDs based on PV[50, 52] and PB[51, 52] with $R_I \sim 0.5$A/W and bandwidth~ 110GHz at 1.55μm for source-drain bias<1V.

Here, we report compact (~0.5-4μm), PTE-based, waveguide-integrated, plasmonic-enhanced GPDs for telecom wavelengths with $R_V \sim 12.2$V/W at zero source-drain bias and zero dark current, with a 3dB cutoff frequency~ 42GHz. To the best of our knowledge, this is the largest R_V to date for waveguide-integrated GPDs operating in voltage mode. We use SLG grown by chemical vapor deposition (CVD) and transferred onto low-loss (~ 1dB/cm) planarized (i.e. fully-embedded in polished cladding[7]) SiN waveguides with a semi-dry (i.e. combining wet de-lamination from the growth substrate with dry lamination onto the target substrate) transfer[86], unlike previous PTE GPDs exploiting non-scalable MC SLG[45, 46]. Our design relies on Au split-gates to electrostatically create a p-n junction in the SLG channel, as well as to guide a confined SPP waveguide mode. By leveraging optical field enhancement and plasmonic confinement in the gap, we increase light-SLG interaction and optical absorption in the p-n junction region, resulting in a confined electrons heat source, compact device length, and increased R_V. This combines high-performance (large R_V, high-speed, bias-free, compact, direct $V_{\rm ph}$ read-out) PTE GPDs in the telecom range with scalable fabrication, paving the way for graphene integrated receivers for next-generation transceivers.

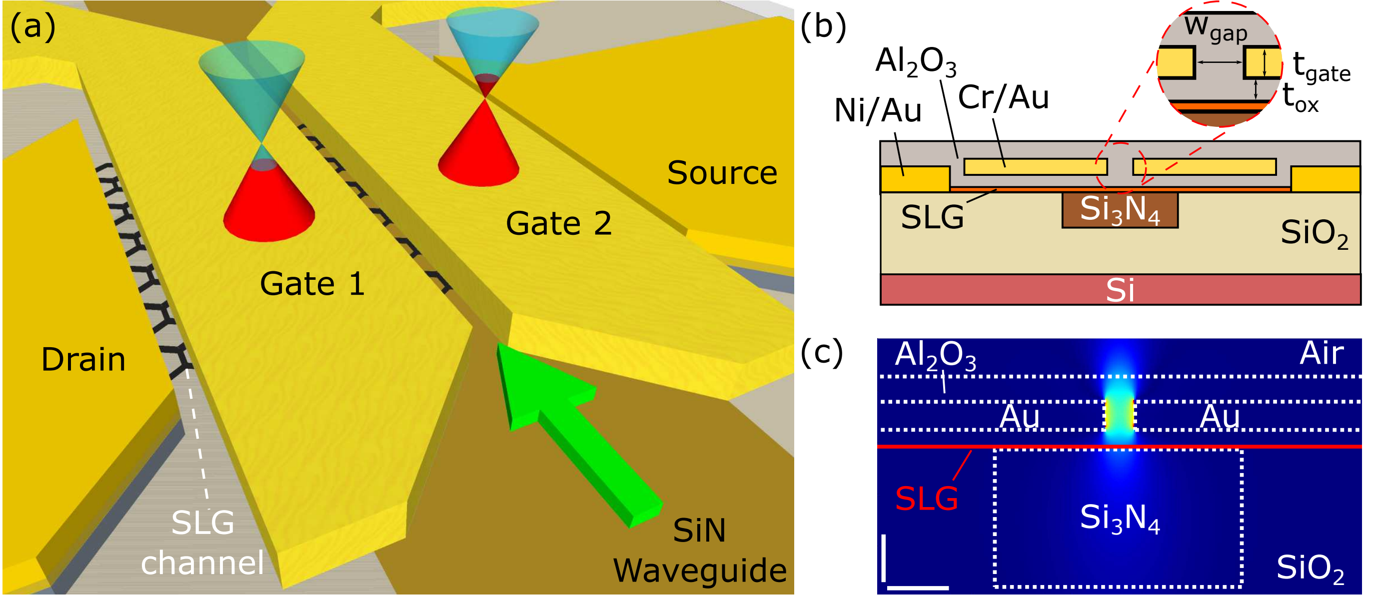

FIG. 1. a) Schematic view of our GPD: SLG on SiN waveguide (brown) with split-gates, acting as plasmonic slot waveguide, to create a p-n junction in the channel (as depicted by the Dirac cones above the gates). The green arrow indicates the light propagation direction. b) Schematic cross-section of the GPD active region. c) Simulated electric field (E_x, in-plane) distribution of the fundamental SPP waveguide mode. For clarity, only the field component parallel to the SLG channel is shown. The vertical and horizontal scale bars are 100 and 250nm

The design of our GPD is schematically shown in Fig.1a,b. It comprises a SLG channel on a SiN waveguide supporting a transverse-electric (TE, in-plane) polarized fundamental waveguide mode. Two Au gates are placed above the channel, separated from the SLG by an Al_2O_3 dielectric spacer and centrally aligned with respect to the waveguide. When this split-gate structure is DC (direct current) biased, it forms a p-n junction, Fig.1a, and creates a S profile in the SLG channel, as for Eq.2. When an on-chip guided light signal reaches the PD area, it is evanescently coupled from the SiN waveguide to the split-gate, which acts as SPP waveguide, Fig.1c. The plasmonic guiding with light confinement in the gap (width $w_{\rm gap}$ ∼100nm) leads to enhanced optical absorption and a localized hot electron distribution with a $T_{\rm e}$ gradient in the p-n junction (gap) region. The coupling efficiency, $P_{\rm out}/P_{\rm in}$, where $P_{\rm out}$ is the power transferred between two optical components, from photonic to plasmonic waveguide mode can be optimized by tailoring $w_{\rm gap}$ and dielectric spacer thickness ($t_{\rm ox}$).

To optimize the cross section parameters at λ=1.55μm, we perform optical simulations using a commercial finite difference solver tool (Lumerical MODE). After selecting the fundamental gap plasmon mode for a given design and λ, we extract the optical electric field distribution in the SLG channel to model the absorbed power density that generates the hot carrier distribution as time-averaged electric power dissipation density[97, 98], which we refer to as Joule heat source (J) hereafter. After normalization to an input power of 1μW, this is used in the heat equation[47, 65, 78]:

$$-\kappa_e(x)\left[\frac{\mathrm{d}^2}{\mathrm{d}x^2}\Delta T_e(x)-\frac{1}{\xi^2}\Delta T_e(x)\right]=J\,(x) \qquad (3)$$

where $\Delta T_e(x) = T_e(x) - T_l$ is the local temperature fluctuation, ξ is the cooling length (see Methods) and $\kappa_e(x)$ is the electronic thermal conductivity (see Methods). Eq.3 gives the $T_e(x)$ profile along the SLG channel. The $S(x)$ profile from Eq.2 is used in Eq.1 to obtain $V_{\rm ph}$. The device parameters are chosen to maximize $V_{\rm ph}$.

A second aspect of device design concerns the coupling between the dielectric and plasmonic waveguides, as well as the positioning and width of the SLG channel along the split-gate. Taper-assisted butt-coupling (end-to-end alignment) was reported to yield the lowest insertion loss (< 0.6dB)[99] for the transition from optical to plasmonic modes. However, since evanescent coupling (lateral or vertical alignment) provides simpler fabrication[100] and greater flexibility for the placement of devices on top of integrated optical circuits[101], we use this here, Fig.1a-c. To obtain the largest R_V, the electric field distribution along the propagation directions needs to be considered. Light absorption in SLG or in the plasmonic structure along the device leads to an exponential decay of optical power[60]. Thus, the increase in T_e follows the same decay. The resulting photovoltage drop at different points along the device results in an averaged potential difference between source and drain contacts. To optimize R_V, a compact (<10μm) device with optimized peak absorption and minimal drop-off is preferable. We thus per-

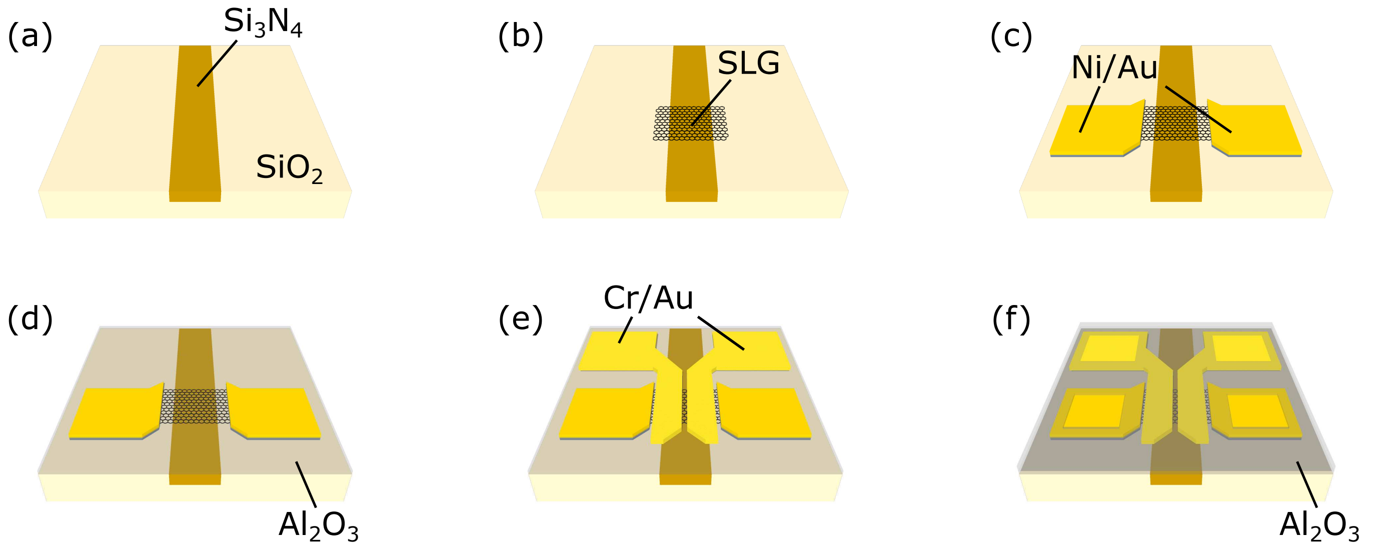

FIG. 2. a) Planarized SiN waveguide. b) SLG transfer and shaping by oxygen plasma etch. c) Ni/Au contacts to SLG channel. d) Al_2O_3 gate oxide deposition. e) Cr/Au evaporation of split-gate structure. f) Al_2O_3 encapsulation and contact pads opening

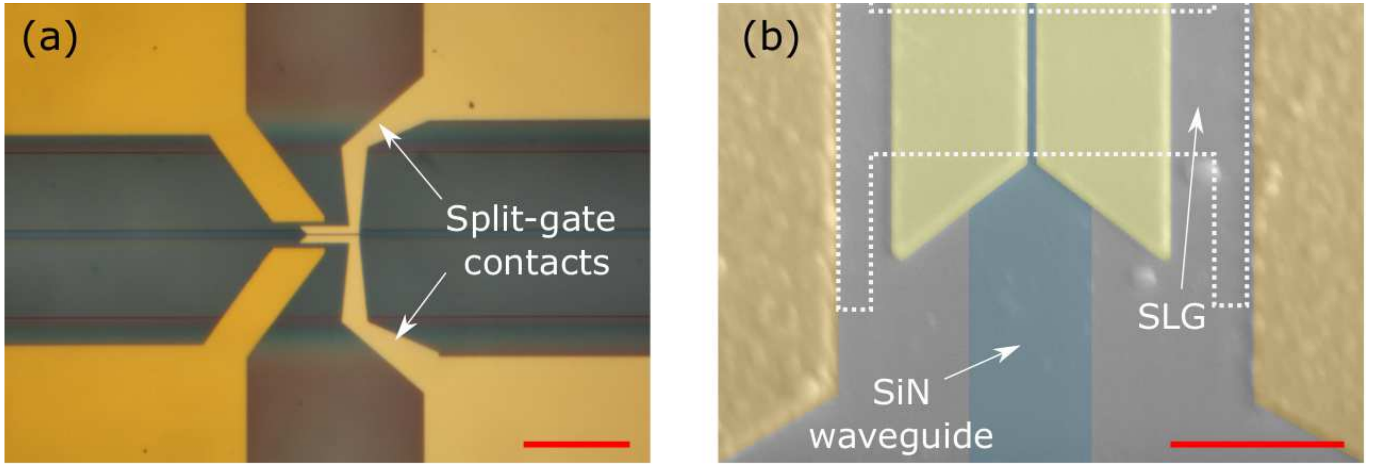

FIG. 3. a) Optical image of a GPD. Scale bar: 20μm. b) Scanning electron micrograph of split-gate. False colors: brown, Ni/Au contacts; yellow, Cr/Au gates; green, planarised SiN waveguide; white dashed line, SLG channel. Scale bar: 2μm

form finite-difference time domain (FDTD) simulations in Lumerical FDTD (see Methods). The co-existence of plasmonic and dielectric waveguide leads to oscillating power exchange between both structures[100–102]. For the highest coupling efficiency, the vertical distance between these waveguides is typically$>$ 150nm[100, 101], exploiting interference between quasi-even and quasi-odd eigenmodes[100–102]. In our design, we keep this separation small (tens nm) to ensure overlap between SLG and gap plasmon mode, to avoid a long ($>$ 5μm) coupling length[100], and to create a sharper concentration of power close to the front of the plasmonic structure. The SLG channel is placed accordingly, after a short ($\sim$1μm) taper at the front of the SPP waveguide to reduce mode mismatch.

Fig.2 summarizes the fabrication process of our GPDs. Planarized SiN waveguides, Fig.2a, (260nm high, width 0.8-1.5μm) on 15μm SiO_2 are fabricated as follows. The SiN layer is first deposited by low-pressure (LP) CVD. The SiN photonic waveguides are then defined by electron beam lithography (EBL) and reactive ion etching. For surface planarization, a 1.6 μm thick boron-phosphorus tetraethyl orthosilicate (BPTEOS) layer is deposited as top cladding and subsequently etched to a final thickness$\sim$ 20nm on top of the SiN waveguides, avoiding chemical mechanical polishing. SLG is grown on pre-patterned, electropolished Cu with Cr nucleation sites as for Ref.[86]. After an initial annealing in argon (10mins), SLG growth is initiated at 25mbar with argon, hydrogen, and methane flowing at 900, 100, and 1 standard cubic centimeters per minute (sccm), respectively. After growth, SLG single crystals are placed onto the

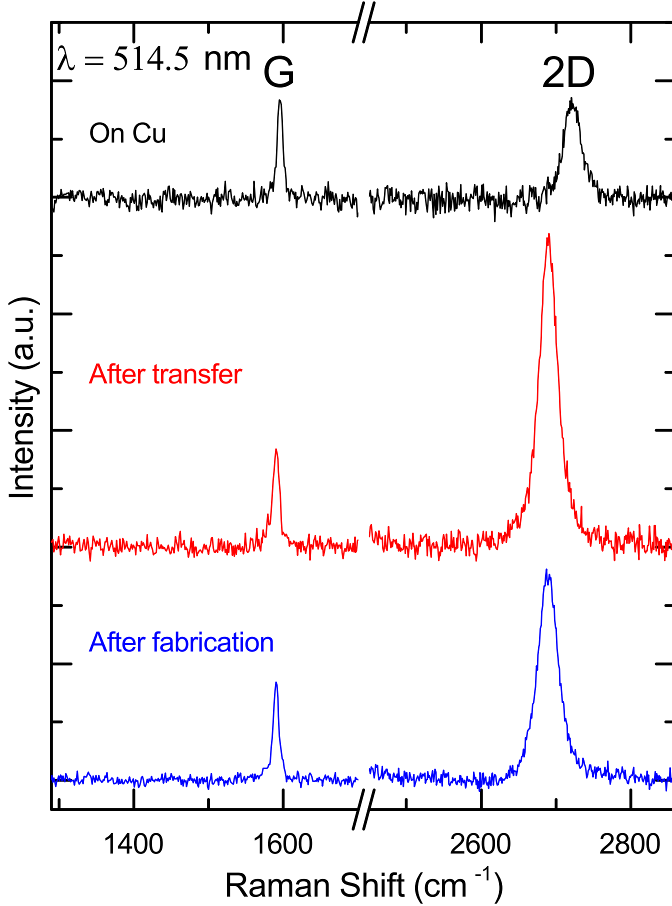

FIG. 4. Raman spectra at 514.5 nm for SLG as grown on Cu (black), after transfer onto the SiN waveguide (red), and after device fabrication (blue). All spectra are normalised to the intensity of the G peak, I(G), and are shown after subtraction of the substrate signals.

photonic chips by semi-dry transfer[86], comprising the spin-coating of a poly(methyl methacrylate) (PMMA) support layer, the attachment of a Kapton frame for handling, electrochemical delamination of SLG in sodium hydroxide, and the lamination onto the target substrate with the help of a micro-manipulator to align the crystals with the photonic structures. A PMMA etch mask is then used to shape the device channel and remove excess SLG over grating coupler and waveguides, defined using EBL. This is followed by oxygen plasma etching at 3W, Fig.2b. Next, contacts are defined by another EBL step. Metallization (15nm Ni/40nm Au) is done by sputtering, thermal evaporation and lift-off in acetone, Fig.2c. 30nm Al_2O_3 is used as gate oxide, via atomic layer deposition (ALD), Fig.2d. An additional EBL step and electron beam evaporation are used to fabricate the plasmonic split gates, Fig.2e. To encapsulate the device and prevent air breakdown in the gap between gate contacts when$\sim$10V is applied, we deposit another 40nm Al_2O_3 by ALD. A laser writer is used to define an etch mask to open access to all contacts, Fig.2f.

The quality of SLG is monitored by Raman spectroscopy at all critical points during the fabrication process, using a Renishaw InVia equipped with a 50x objective (numerical aperture NA=0.75) at 514.5nm with power below 0.5mW to exclude heating effects and risk of damage. Representative spectra of SLG on Cu (after removal of Cu background photoluminescence[103]), after transfer onto the waveguide, and after complete device fabrication, are shown in Fig.4. The absence of a D peak confirms negligible defects are introduced during fabrication. The 2D peaks are single-Lorentzian, confirming the presence of SLG[104, 105]. On Cu, the position and full width at half-maximum of the G peak are Pos(G)$\sim$1595cm^{-1} and FWHM(G)$\sim$ 8cm^{-1}. The position of the 2D peak, Pos(2D), is$\sim$2721cm^{-1} with FWHM(2D)$\sim$27cm^{-1}. The 2D to G peak intensity, I(2D)/I(G), and area, A(2D)/A(G), ratios are$\sim$ 1 and$\sim$ 3.2. After transfer, Pos(G)$\sim$ 1590cm^{-1}, FWHM(G)$\sim$10cm^{-1}, Pos(2D)$\sim$ 2690cm^{-1}, FWHM(2D)$\sim$28cm^{-1}, I(2D)/I(G) $\sim$ 3.2 and A(2D)/A(G) $\sim$ 8.6. This corresponds to$\sim$ 250meV doping[106, 107] and a carrier concentration$\sim$4$\times$10^{12}cm^{-2}. After the final encapsulation, Pos(G)$\sim$1590cm^{-1}, FWHM(G)$\sim$9cm^{-1}, Pos(2D)$\sim$2689cm^{-1}, FWHM(2D)$\sim$30cm^{-1}, I(2D)/I(G) $\sim$ 2.2 and A(2D)/A(G) $\sim$ 7.6, indicating$\sim$350meV ($n \sim 7\times10^{12}$cm^{-2}) doping.

To determine the DC operating point, we perform electrical characterizations by sweeping the split-gate voltages ($V_{\text{Gate }1}$, $V_{\text{Gate }2}$) while measuring the device current I_{DS} under a constant source-drain bias V_{DS}=1mV, using DC probes on micromanipulators and two source measure units. To record the static photoresponse, we add two fibre probes and couple continuous wave (CW) transverse-electric (TE) polarized light at 1.50-1.58μm from a tunable laser into the SiN waveguide via an optical fibre and a grating coupler (GC). While V_{ph} is recorded across the unbiased (V_{DS}=0V) channel as a function of $V_{\text{Gate }1}$ and $V_{\text{Gate }2}$, using a lock-in amplifier under internal modulation (square wave, ON-OFF) of the laser with 200Hz, we monitor the transmission with a second fibre positioned over the output GC and connected to an external InGaAs power meter to ensure constant P_{in}.

Fig.5a plots the R map of a typical device as a function of $V_{\text{Gate }1}$, $V_{\text{Gate }2}$. This shows a four-fold pattern, corresponding to the four doping constellations (p-n, n-p, n-n, p-p) in the SLG channel for different combinations of gate voltages. The map is symmetric with a maximum R $\sim$9kΩ at the crossing of the charge neutrality point (CNP), between -4 and -5V. This corresponds to n-doping of the unbiased SLG channel with n$\sim$7$\times$10^{12}cm^{-2} ($\sim$350meV). R has contributions from channel (R_{ch}) and contact (R_c) resistances. R_{ch} includes a fixed contribution from ungated SLG regions and a gate-dependent contribution from channel segments underneath the split-

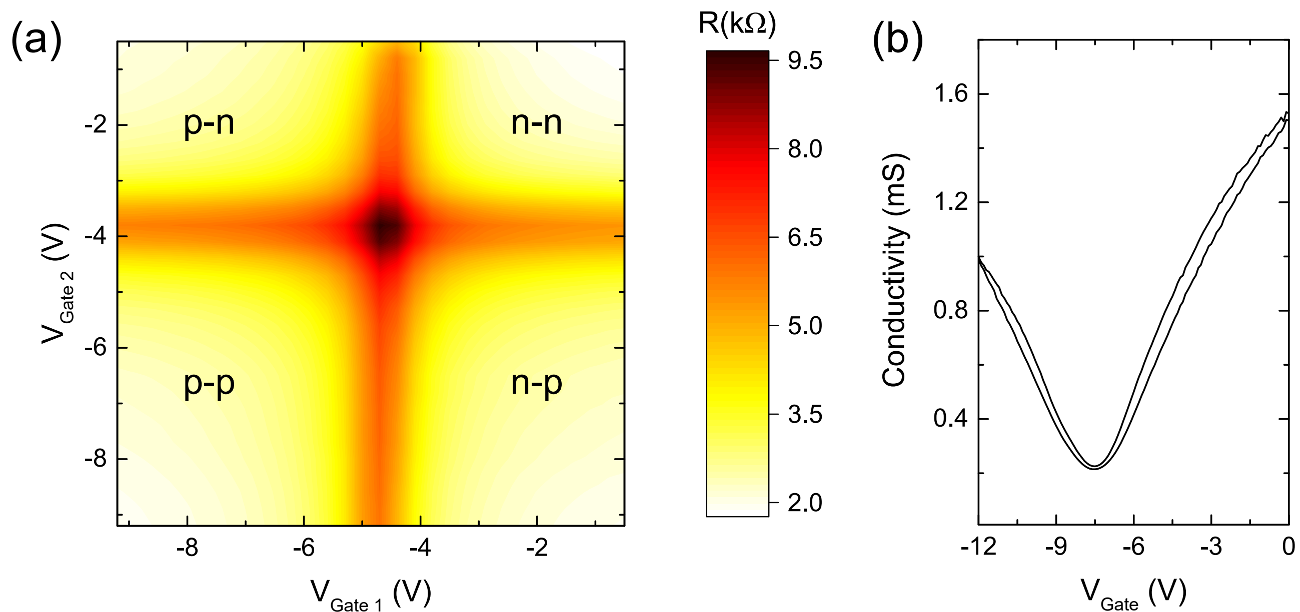

FIG. 5. (a) GPD channel resistance as function of split-gate voltages. (b) Conductivity vs. gate voltage from a 4-terminal measurement on test Hall bars

gates. The gate-dependent variation in R in Fig.5a suggests R_{ch} as the dominant factor. This is consistent with our contact resistivity (<1k$\Omega\mu$m) for CVD SLG and the calculated R based on channel geometry and sheet resistance obtained from independent four-terminal measurements on reference Hall bars. From these we also extract an average μ ~2000cm^{2}V^{-1}s^{-1} from linear fits of the conductivity via[108] $\mu = |\mathrm{d}\sigma/\mathrm{dV_{Gate}}|/C_{\rm ox}$, where $C_{\rm ox}$ is the top gate capacitance. Fig.5b is a bi-directional gate sweep of the conductivity, indicating low hysteresis and charge-trapping in the Au/Al_2O_3/SLG gate capacitor.

Fig.6a is a $V_{\rm ph}$ map of a typical device at $P_{\rm in} \sim 100\mu$W inside the GPD. The plot exhibits a six-fold pattern with higher response for bipolar (p-n, n-p) junctions and a weaker one with sign-crossing along the diagonal ($V_{\rm Gate\ 1} = V_{\rm Gate\ 2}$) for the unipolar (n-n, p-p) junctions. When the GPD is operated at zero V_{DS}, this indicates a PTE-dominated photodetection as the two sign changes in $V_{\rm ph}$ along a single-gate sweep line (e.g $V_{\rm Gate\ 2}$ =const.) reflect the two sign changes of the S gradient across the junction, arising from the non-monotonic dependence of S on μ_c[65]. The measured photoresponse is in good agreement with the calculated one in Fig.6b. We observed a similar behavior on> 12 devices of different sizes across 5 chips, the shortest being 500nm in the light propagation direction for a footprint~3μm^2. For all devices, we got a maximum $V_{\rm ph}$ close to the CNP where S is largest, with a gradual drop-off at higher doping.

To calculate R_V, we first estimate the optical power inside our GPDs by taking into account: a) combined loss (~9.6dB at peak transmission) of waveguide propagation and fiber-to-waveguide coupling (wavelength-dependent, following the response envelope of the GC); b) 3dB power reduction from the input laser modulation (square wave, ON-OFF) with a 50% duty cycle; c) 3dB power splitting in the Y-branches and their~0.2dB losses. We get R_V ~ 12.2V/W, the largest reported so far for waveguide-integrated GPDs in voltage mode at zero-bias.

Fig.6c plots the R_V wavelength dependence, showing a broadband (1.50-1.58μm) photoresponse covering the entire C-band (1.53-1.565μm[109]) and beyond. The error bars indicate variations in the wavelength-dependent coupling loss (thus $P_{\rm in}$), estimated as standard deviation from transmission measurements on>10 reference waveguides. We attribute the gradual increase in R_V with increasing wavelengths to improved coupling efficiency from dielectric to plasmonic waveguide.

Fig.6d is the $V_{\rm ph}$ power dependence at 1.575μm for optical power levels comparable to those required by receivers used in 100GBs^{-1} links[32]. The linear response indicates a power-independent R_V.

To highlight our GPDs' behavior as voltage sources, when a signal is generated, we place two devices back to back on the same waveguide and connect them in series. This modified design, Fig.7a, consists of two SLG channels gated from the same split-gate/SPP waveguide. By connecting the drain pad of one channel to the source of the other through a metal lead crossing the waveguide behind the active region of the devices, Fig.7b, we measure both GPDs individually, as well as combined. Fig.7c is a false color SEM of the active region of both detectors. Since each GPD is designed to maximally absorb over the device length, the power rapidly decays along the propagation direction after the first GPD. We thus

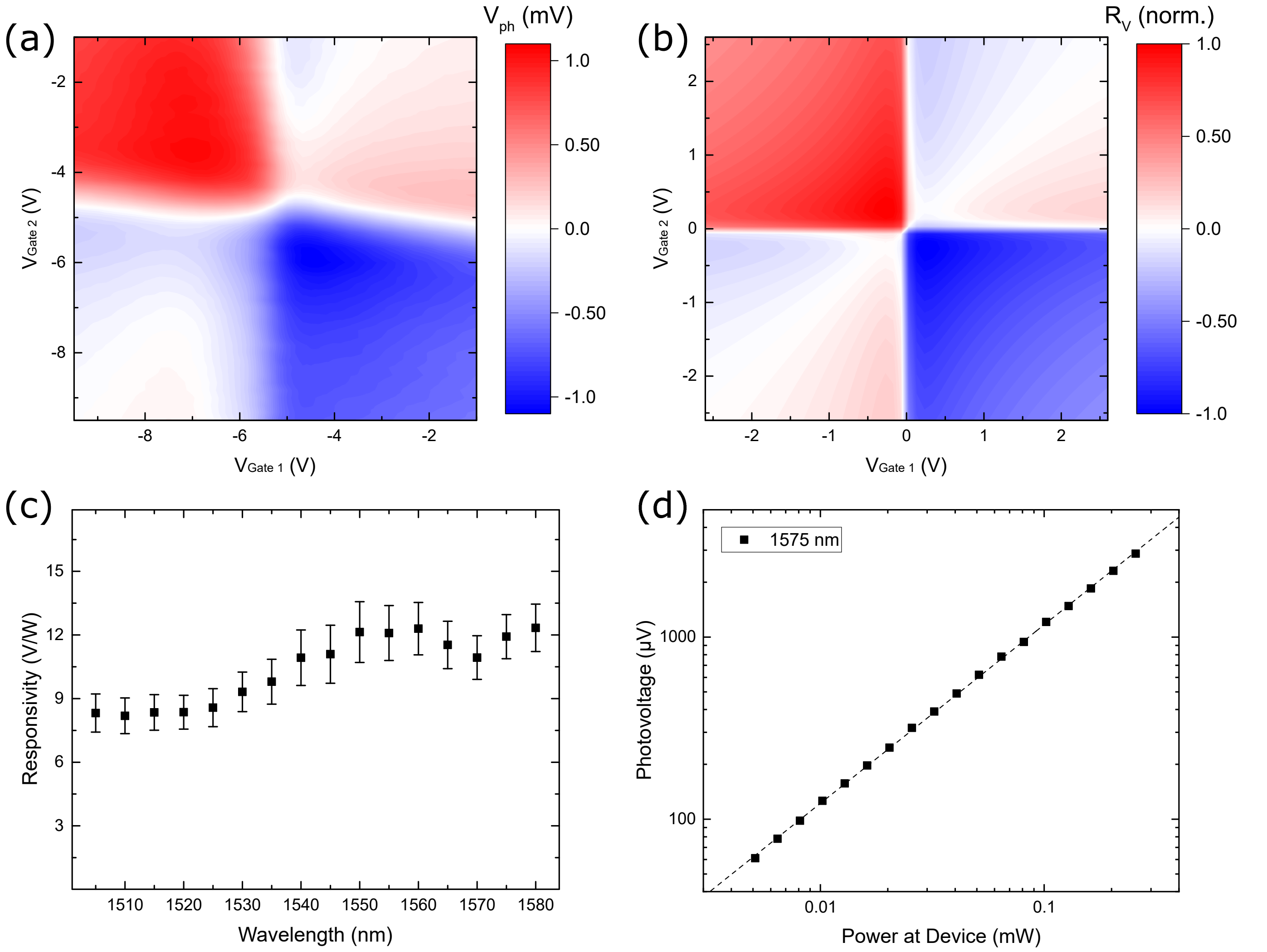

FIG. 6. a) Experimental photovoltage map for zero bias. b) Simulated responsivity. c) Wavelength dependence of responsivity. d) Power dependence of responsivity at 1575 nm.

place the second device$\sim 1\mu$m from the first.

Figs.7d,e plot the photovoltage maps for both GPDs at $P_{\rm in} \sim 70\mu$W. The GPD closer to the input GC (A) absorbs most of the light and has the six-fold pattern typical of PTE, Fig.7d. The photoresponse of the second GPD (B) is weaker, due to light absorption in SLG and metal, Fig.10d,e. A six-fold pattern is not observed, due to photocurrents generated in the junctions between gated and ungated sections at either end of the SLG channel. Figs.7f,g are photovoltage maps of the combination of both GPDs. The response in series is in Fig.7f, while the sum of the individual responses in Fig.7g. The two plots are good agreement, confirming that $V_{\rm ph,A+B} = V_{\rm ph,A} + V_{\rm ph,B}$. Thus, in order to increase R_V in long (tens μm) PTE-GPDs with absorption only in the SLG channel, one could avoid the reduction in photosignal due to the decrease in ΔT_e along the device and instead add the voltages generated in different sections by subdividing the channel into several shorter devices and connecting them as cascaded GPDs. To minimize the length of metal leads for contacting and connecting individual devices, this configuration could comprise individually gated devices with alternating p-n junctions to form a meandered structure. This would ideally be implemented with transparent gates, such as indium tin oxide, or a second SLG at a distance far enough from the channel, to avoid additional losses.

To evaluate the frequency response we use the optical heterodyne set-up in Fig.8a, combing optical signals at different frequencies. The channel is contacted with an RF probe in G-S configuration. The output of our tunable laser source is combined with that of a fixed-wavelength laser diode (Thorlabs SFL1550P) and the GPDs' response to the amplitude beating at the difference frequency is monitored with an electrical spectrum analyzer (ESA, Agilent PSX N9030A). The two source

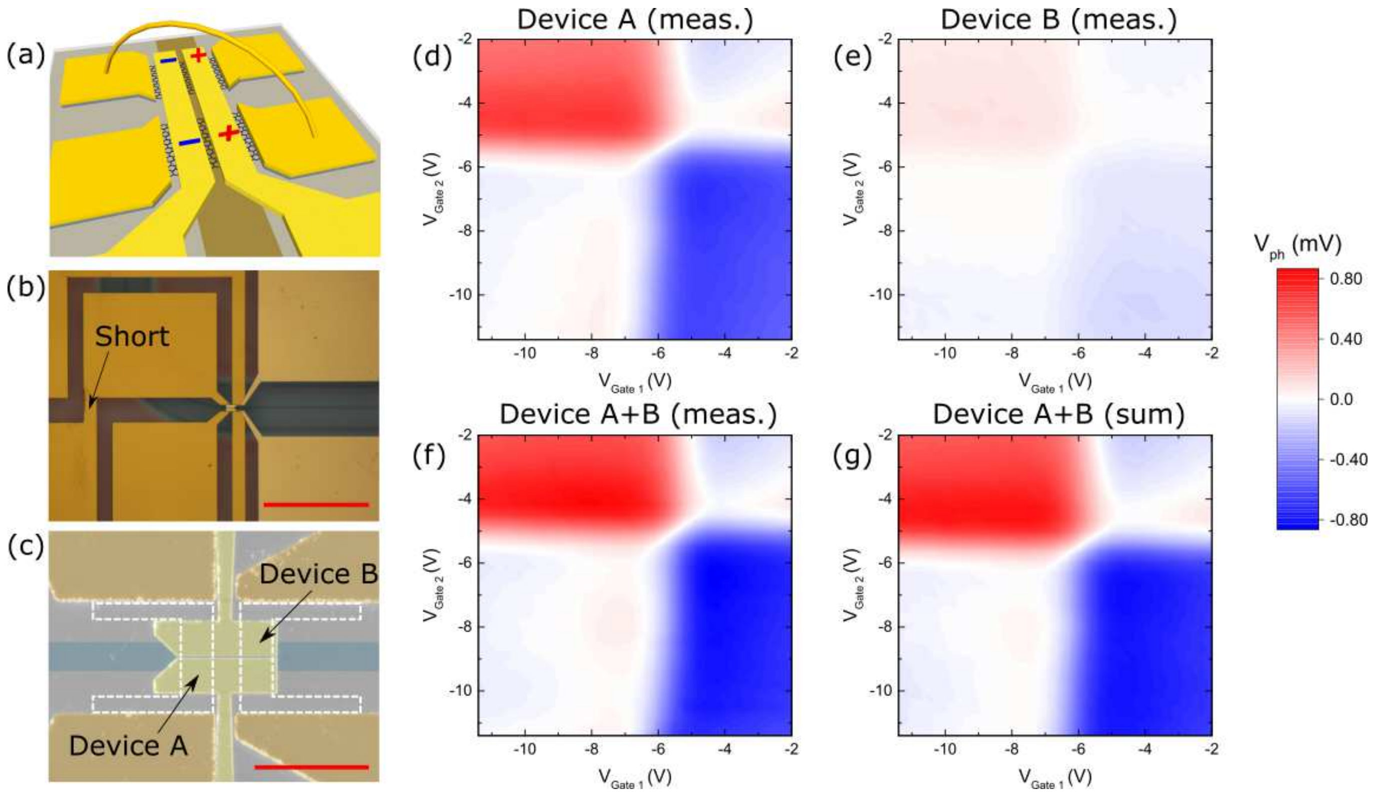

FIG. 7. a) Schematic of test structure to measure two GPDs in series. b) Optical image of contact pad short to connect both GPDs in series. Scale bar: 80μm. c) SEM image of active region of test structure. False colors: brown, Ni/Au contacts; yellow, Cr/Au split gate; green, planarized SiN waveguide. The SLG channels are indicated by white dashed lines. Scale bar: 5μm. d) Photovoltage map of device A at the start of the SPP waveguide. e) Photovoltage map of device B at the end of the SPP waveguide. f) Photovoltage map of devices A and B in series. g) Sum of the photovoltage maps for devices A and B

outputs are combined in a 50:50 fibre coupler. We monitor the signal stability (i.e. output power and the position of the difference frequency) using a reference PD and an oscilloscope. Prior to coupling the combined signal into the SiN waveguide, we use an erbium-doped fibre amplifier (EDFA, Keyopsys CEFA-C-HG) to raise the optical power to 15dBm (∼30mW) to increase the output signal detected at the ESA. To overcome the signal reduction due to impedance mismatch between device R and the 50Ω of the measurement equipment, we use an additional low noise amplifier (LNA) between GPD and ESA. In order to distinguish between the frequency response of our GPDs and that of the LNA and the remaining measurement equipment, the response of the latter two to a low power (-80dBm) input from a 50GHz signal generator is recorded for calibration.

Fig.8b plots the calibrated response (black squares) to the beating signal at different frequencies, while the split-gate is biased to set an operating point in the p-n junction regime resulting in the largest photoresponse under CW illumination in Fig.6. The response stays within 3dB of the low-frequency (1GHz) reference power until 40GHz, the limit of our measurement set-up.

To determine the cut-off, we therefore modify the set-up (Fig.8c) to perform impulse response measurements, where the response to ultra-short (∼150fs) optical pulses is monitored with an oscilloscope. For excitation, we use the idler of an optical parametric oscillator, pumped by a Ti:Sa mode-locked laser at 1.55μm, attenuated in free-space prior to coupling into the optical fibre. Fig.8d is the measured impulse response at the same operating point as for the heterodyne measurements. We obtain a pulse duration, assuming a Gaussian pulse shape, $\Delta t \sim 11$ps. For Gaussian-shaped pulses, the time-bandwidth product is∼0.44[110]. From this we estimate a $f_{3\mathrm{dB}} \sim 0.44/\Delta t \sim$ 40GHz. The fast Fourier transform of the pulse is in Fig.8b (red circles) after calibration. The trace is in good agreement with the heterodyne response and drops below -3dB at∼ 42GHz, showing high-speed operation on par with current Ge PDs, consistent with other reports of high-speed MC-SLG-based PTE GPDs[45–47]. However, this bandwidth is the highest reported so far for PTE-based on-chip GPDs made from CVD SLG.

In summary, we reported waveguide-integrated plasmonic enhanced GPDs with an external responsivity∼12.2V/W, a -3dB cut-off∼42GHz, and small (∼3-20μm^2) device footprints, using CVD SLG on SiN. We exploited the integration of an SPP waveguide

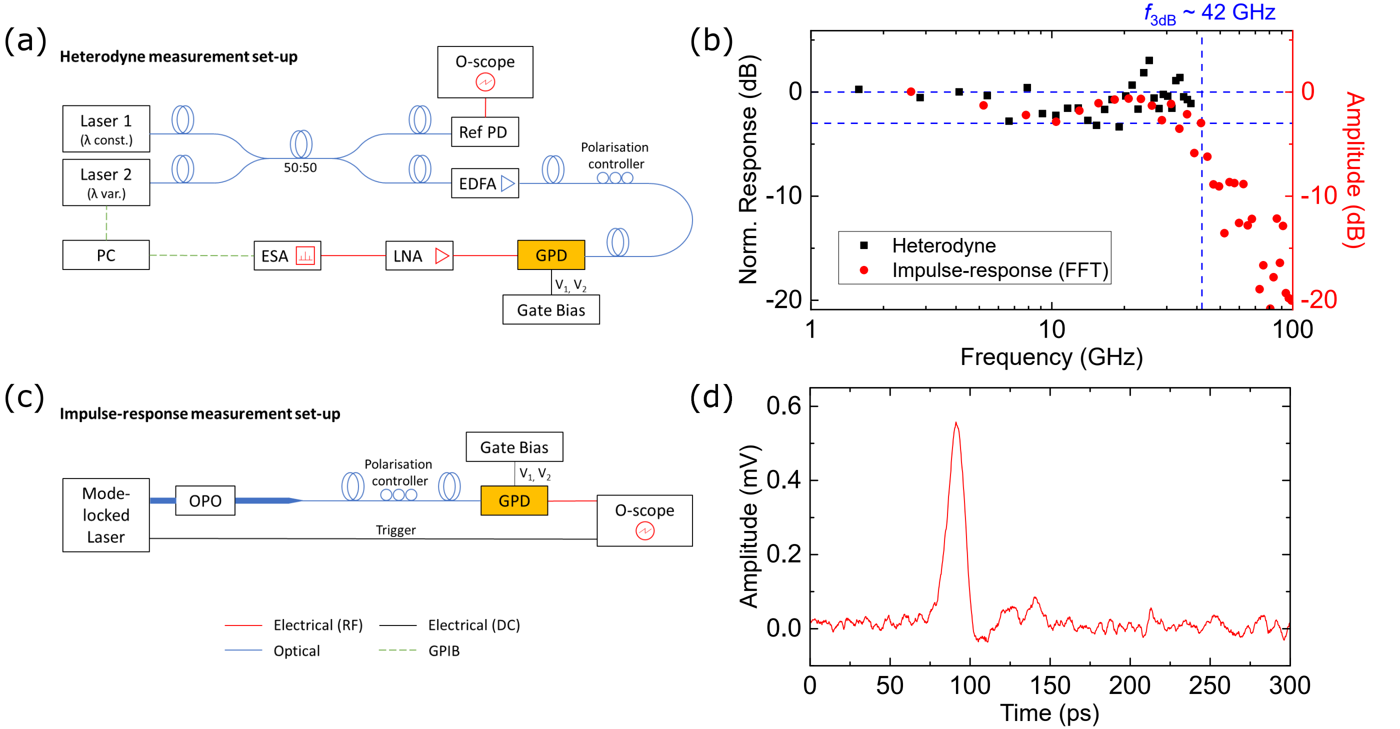

FIG. 8. a) Schematic heterodyne set-up. b) Frequency response at zero V_{DS} from (black) direct heterodyne measurement and (red) fast Fourier transform of impulse response. c) Schematic impulse-response measurement set-up. d) Impulse-response for~150fs optical pulses at zero V_{DS} and p-n gate bias.

with a SLG p-n junction to enhance light-SLG interaction and create a confined electron heat-source to obtain a strong, PTE-dominated photoresponse. This paves the way to power-efficient receivers for optoelectronic links.

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METHODS

Device design and modeling

Plasmonic gap width, SLG placement, and thickness of metal and oxide structures are the key parameters to be optimized to achieve maximum photovoltage. To do so, we build a device model in the layout environment of a commercial eigenmode solver (Lumerical MODE Solutions). In order to model SLG in the optical solver and subsequent calculations consistently, we use a volumetric permittivity material model, in which SLG is described as cuboid with finite thickness $t = 0.34$nm and in-plane ($\varepsilon_{\parallel}$) and out-of plane ($\varepsilon_{\perp}$) permittivity are defined as independent tensor elements. To calculate the in-plane relative permittivity for SLG, we use[111]:

$$\varepsilon(\omega) = \varepsilon'(\omega) + i\varepsilon''(\omega) = \varepsilon_r + \frac{i\sigma(\omega)}{\varepsilon_0 \omega t} \quad (4)$$

where $\varepsilon'(\omega)$ and $\varepsilon''(\omega)$ are the real and imaginary part of the relative permittivity $\varepsilon(\omega)$, $\sigma(\omega)$ is the SLG optical conductivity, ω is the angular frequency, ε_r is the background relative permittivity (whose frequency-dependence is ignored in the small (λ =1.5-1.6μm) wavelength range under consideration), and ε_0 is the permittivity of free space. $\sigma(\omega)$ is obtained by linear-response[112] in the random-phase approximation[111], and contains terms describing intraband and interband transitions. While the former can be evaluated analytically[112], the interband term requires a numerical solution[111, 112]. The out-of-plane component of the dielectric tensor matches ε_r.

We then run the eigenmode solver, using the relative permittivity function for SLG, and select the fundamental (gap plasmon) mode for further processing. We export the simulation mesh grid positions, electric **E** and magnetic **H** data, effective refractive index ($n_{\text{eff}} = \beta/k_0$, where β is the propagation constant of the mode and k_0 is the free space wavevector[113]), and all relevant geometric parameters such as gap and gate width and gate oxide thickness to complete the rest of our modeling.

A crucial intermediate step requires the determination of the $T_e(x)$ profile in the SLG channel. The first step establishes the operating regime. As discussed in Refs.[114, 115], the energy delivered to the electronic carrier distribution by pumping SLG with a pulsed laser can

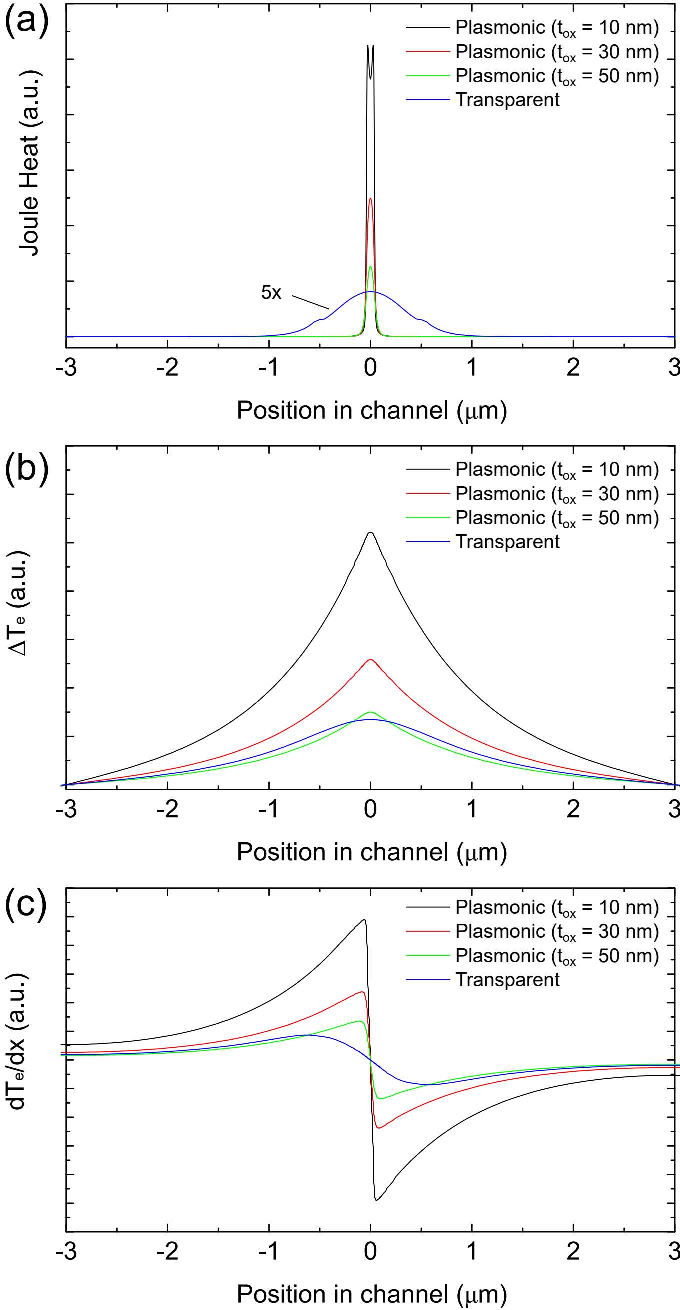

FIG. 9. a) Joule heat source, b) T_e profile, c) $\frac{dT_e}{dx}$ along SLG channel for a representative GPD with plasmonic gates at different heights above the channel compared to gates transparent at 1.55μm

be sufficiently high to result in $T_e(x) > 1000$K. When modeling photoexcited SLG under these conditions, one has to take into account the $T_e(x)$ dependence[114, 115] of all thermodynamic and transport parameters in Eqs.1-3, i.e. μ_c, $\sigma(x)$,$\kappa_e(x)$, resulting in a nonlinear system of coupled equations.

The contrasting case, the "weak heating" regime, is characterized by $|\Delta T_e(x)| \ll T_l$[62, 81]. Under this condition, Eqs.1-3 can be solved to linear order in the local $T_e(x)$ fluctuation, evaluating all thermodynamic and transport parameters at $T_e(x) = T_l$. In particular, a single μ_c is established, following photoexcitation, by electron-electron interactions across the valence and conduction bands, and the thermal conductivity, calculated from the Wiedemann-Franz law $\kappa_e = \pi^2 k_B^2 T_e \sigma/(3e^2)$[74], is uniform in space.

The intended operation of our GPD is under CW or, during data reception, quasi-CW (i.e. the pulse duration exceeds the cooling time of the hot-carrier distribution) illumination with low $P_{\rm in} < 0.1$mW at in-plane incidence. Furthermore, a linear dependence of $V_{\rm ph}$ on $P_{\rm in}$, such as in Fig.6d, is observed[62]. We thus conclude that our device operates in the "weak heating" regime.

In order to evaluate Eq.3, we need to specify the cooling length ξ and the light absorption heat source. In principle, ξ, which describes the energy transfer from the electronic system to the optical phonons[65], depends on $T_e(x)$ and n. However, under the "weak heating" regime, the $T_e(x)$ dependence can be neglected, and n is uniform in the device (with opposite sign in the two regions of the p-n junction) when the photoresponse is maximal. For these reasons, in our calculations, we assume a constant $\xi = 1\mu$m, consistent with experimental values[47, 78]. $J(x)$ is calculated from the simulated electric field data as the time average of the electric power dissipation density[97, 98]:

$$J(x) = \frac{1}{2}\omega\epsilon''|\mathbf{E}|^2 = \frac{1}{2}\frac{\sigma}{t}\mathbf{E}\cdot\mathbf{E}^* \tag{5}$$

In order to relate $J(x)$ to physically meaningful quantities, we integrate the normal component of the time-averaged Poynting vector over the simulation region and normalize it to a given input power.

After solving Eq.3 for the $T_e(x)$ fluctuation profile $\Delta T_e(x)$, we take its derivative with respect to x and obtain the second factor of the integrand in Eq.1. Figs.9a-c compare the absorption heat source, the resulting $T_e(x)$ profile, and its derivative for a representative GPD in presence of a plasmonic split-gate at different heights over the SLG channel, to an unperturbed fundamental dielectric waveguide mode, where the p-n junction is generated by a transparent (at the chosen λ) gate, such as a split-gate made from a second SLG at a separation large enough to avoid additional optical losses. The beneficial role of plasmonic enhancement, with all other parameters fixed, for a sharper increase in $T_e(x)$ translates to larger $V_{\rm ph}$ if the SLG channel is kept close to the SPP waveguide (<50nm).

To model S along the channel, we assume that the structure is gated to achieve the maximum S below the gates, as for Eq.2 (opposite in sign but equal in magnitude for the p-n case) and approximate the gap region with a linear interpolation between the two. Combining both factors in Eq.1 and computing the integral yields

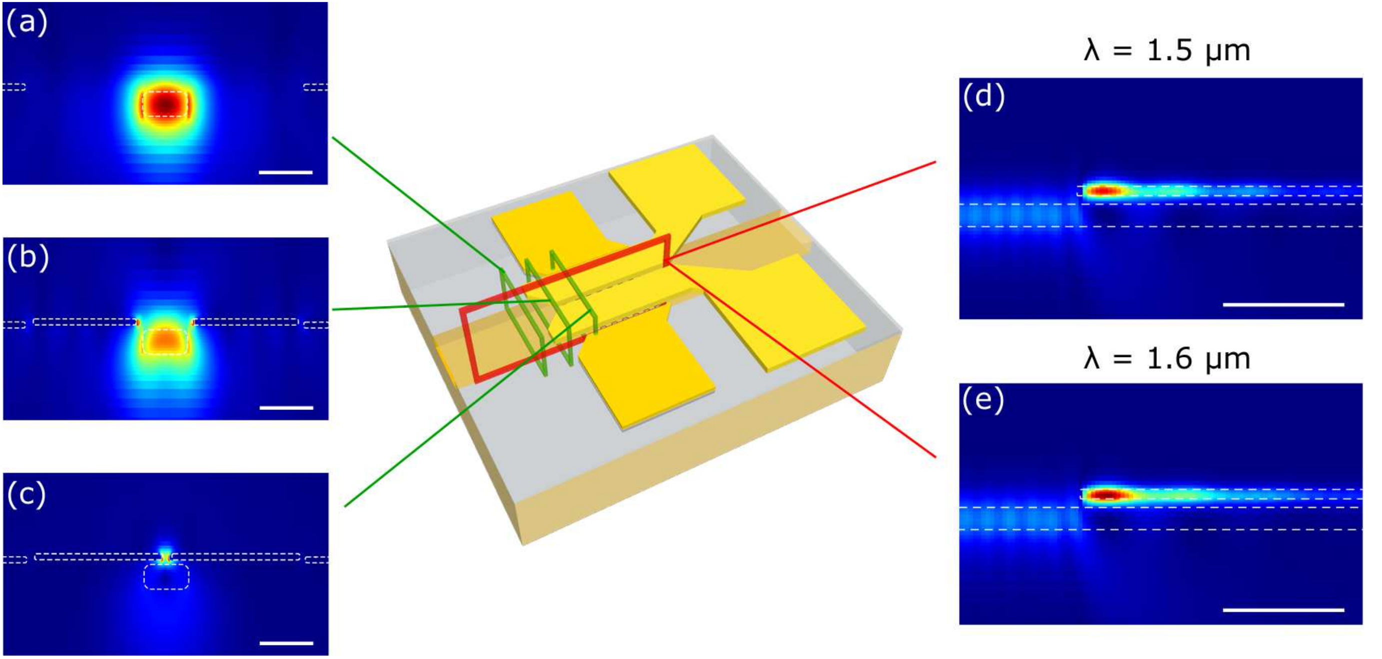

FIG. 10. Field distribution a) before the GPD, b) during transition, and c) start of the split-gate/SPP waveguide. Scale bar: 1μm. (d,e) $|\mathbf{E}|^2$ along the center (red box) of dielectric waveguide and GPD at d)1.5μm and e) $= 1.6\mu$m. Scale bar: 3μm

$V_{\rm ph}$ or R_V (if divided by $P_{\rm in}$) as figure of merit to assess different cross section designs:

$$R_V = \frac{|V_{\rm ph}|}{P_{\rm in}} = \frac{1}{P_{\rm in}}\left| \int S(x)\frac{{\rm d}T_e(x)}{{\rm d}x}\,{\rm d}x \right| \qquad (6)$$

To calculate R_V or photovoltage maps as in Fig.6b, we first generate the S profile for all voltage combinations and then proceed via Eqs.6 or 1.

We then perform a sweep of gap width, SLG position, gate oxide thickness, gate contact height as a function of μ in SLG and ε_r. As for Fig.9, shorter distances between SLG channel and SPP waveguide yield larger signals. Furthermore, the SPP waveguide width affects the expected photovoltage in two ways. 1) narrower confinement improves the field strength at the SLG channel and R_V at the cost of higher propagation losses; 2) the ungated SLG at the center of the device with not maximum S shrinks with smaller gaps. The device parameters are then chosen based on these trends, taking into account fabrication complexity, robustness to processing-induced deviations (e.g. suppression of fundamental gap plasmon mode below a certain gap width), reliability (e.g. oxide break-down) and outcomes of FDTD simulations on coupling and propagation.

Extracting $\mathbf{E}$ and $\mathbf{H}$ of the fundamental mode in the hybrid region is sufficient for the design of the device cross-section. However, it does not capture the field distribution along the device, since optical losses, transition from dielectric to plasmonic waveguide, and power exchange between different modes that co-exist in the hybrid region remain unaccounted for. To find a good combination of SLG position and width within the constraints of the cross-section design, targeting a T_e distribution with maximal derivative across the PD, but minimal along the propagation direction over the device length, we perform FDTD of the transition between SiN waveguide and GPD. We construct a device model in the same way as for the eigenmode analysis and adjust the source settings to 1.5-1.6μm. We launch the fundamental quasi-TE mode of the SiN waveguide towards the GPD and use frequency domain field monitors (FDFM) with various orientations (parallel and perpendicular to the propagation direction) to track the field and power profiles at different points. Figs.10a-c plot the field at 3 cross-sections of a representative GPD. We see transitions from injected mode in dielectric waveguide to field distribution resembling the fundamental gap plasmon.

Figs.10d,e display the electric field intensity from a vertical FDMD monitor along the center line of the GPD, at two wavelengths. As expected for this non-adiabatic transition with fast decrease ($<1\mu$m) of the taper cross-section down to the target gap size, scattering and reflections at the start of the hybrid region reduce the power at the GPD, but the desired sharp intensity profile over length scales that match the fabricated SLG channel widths is achieved. Consequently, we place the SLG channel 100nm after the SPP structure has reached its final gap width. The comparison of field intensities for 1.5 and 1.6μm on the same color scale in Figs.10d,e reveals a larger peak intensity and a longer interaction length for the latter, which indicates improved coupling efficiency at larger λ, as for the wavelength-depended R_V in Fig.6c.

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