Design and preliminary detector performance of the PET component of the TRIMAGE PET/MR/EEG scanner

Nicola Belcari†, *Member, IEEE,* Maria Giuseppina Bisogni, Niccolò Camarlinghi, Pietro Carra, Piergiorgio Cerello, Matteo Morrocchi, Alessandra Patera, Giancarlo Sportelli, *Senior Member, IEEE* and Alberto Del Guerra, *Life Fellow, IEEE*

Abstract— The TRIMAGE project aims at developing a brain-dedicated PET/MR system able to perform simultaneous PET and MR acquisitions for application in schizophrenia. Both PET and MR components have been designed in this project. The PET component consists of a full ring with 18 sectors each comprising three square detector modules. The modules are based on dual-layer staggered matrices of LYSO crystals read out by silicon photomultipliers. The FOV of the combined PET/MR/EEG system has an inner diameter of 260 mm and an axial extension of 160 mm. This paper describes in full detail the final version of the PET detectors and the related electronics. It also reports on the preliminary performance of a pair of sectors in terms of pixel resolvability index (RI), energy resolution, singles count rate capability and coincidence time resolution (CTR). The procedures used for the optimization and calibration of PET detector are described. Results demonstrate the pixel/layer identification performance with a RI of about 0.2 while the energy resolution resulted in 20% and 22% FWHM for the bottom and top layer, respectively. The maximum singles count rate of a PET detector is about 700 kcps and the CTR of two sectors is 515 ps.

***Index Terms*— TRIMAGE project, PET/MR/EEG, PET/MR, Brain PET, Molecular imaging.**

I. Introduction

PET, MRI and EEG can provide complementary metabolic, anatomical, physiological and functional information about the brain. When using separate imaging systems, the integration of information obtained with each modality can be done through combined analysis of the sequentially acquired data by, e.g., using methods for software image co-registration. Alternatively, the multiple modalities can be integrated to run simultaneously within a single multi-modal scanner. This approach is available today either in the form of whole-body PET/MR systems coupled with MR-compatible EEG caps, or with brain-dedicated PET insert prototypes, developed and tested on MRI scanners that were already installed and available for clinical use [1]–[5]. The PET insert approach proved to achieve better performance in terms of spatial resolution and sensitivity with respect to whole body PET/MR systems [1], [6]. Moreover, it allows to reuse already available MRI instrumentation thus reducing the cost of upgrade. The main design challenge for a MR-compatible PET insert is mainly related to the requirements in terms of compactness and MR compatibility [7].

The achievement of compact and MR compatible detectors was enabled by the use of solid-state photodetectors. Except for the first developed system [1] based on avalanche photodiodes (APDs), all the other prototypes use silicon photomultipliers (SiPMs) as photosensors for scintillating crystal readout (LYSO in all cases). The relatively small bore size, if compared with the size of a whole-body PET system, makes the capability of the detector to estimate the depth of interaction (DOI) a real need for mitigating the parallax error. In fact, most recent prototypes are featuring some sort of DOI estimation by using layered [4] or monolithic crystals [5]. Different methods are also used for extracting the signals from SiPMs ranging from a solution where all the readout electronics is located outside the MR bore [2] to others where preamplifiers and readout circuitry are placed right behind the SiPMs and typically enclosed in a shielded cassette [3]–[5]. In all cases, SiPM outputs are multiplexed for reducing the number of readout channels. The typical spatial resolution of the prototypes developed so far is in the 1.6 mm – 3.0 mm FWHM range while the highest sensitivity at the center of the FOV is 7.2% [1].

The advantages of simultaneous multimodal PET/MRI/EEG rely on complementing the structural and functional information of MRI with the temporal dimension provided by EEG and the molecular sensitivity offered by PET [8].

The TRIMAGE project [9] aims to create a brain-dedicated PET/MR system able to perform simultaneous PET and MR acquisitions (Figure 1). Both PET and MR components were custom designed for the purpose and differently from the insert approach they feature a native mechanical compatibility. With the addition of an MR-compatible EEG system, the TRIMAGE system can offer a trimodal imaging capability.

N. Belcari (e-mail: nicola.belcari@unipi.it), M.G. Bisogni, N. Camarlinghi, P. Carra, G. Sportelli and A. Del Guerra are with the Dipartimento di Fisica "E. Fermi", Università di Pisa, 56127 Pisa, Italy and with the Istituto Nazionale di Fisica Nucleare, Sezione di Pisa, 56127 Pisa, Italy.

Matteo Morrocchi, is with the Istituto Nazionale di Fisica Nucleare, Sezione di Pisa, 56127 Pisa, Italy.

P. Cerello and A. Patera are with the Istituto Nazionale di Fisica Nucleare, Sezione di Torino, 10125 Torino, Italy.

This work was supported by the European Union Seventh Framework Programme (FP7/2007-2013) under Grant 602621- TRIMAGE.

Authors declare to have the full control of the data presented in the paper.

We have no other conflicts of interest to disclose.

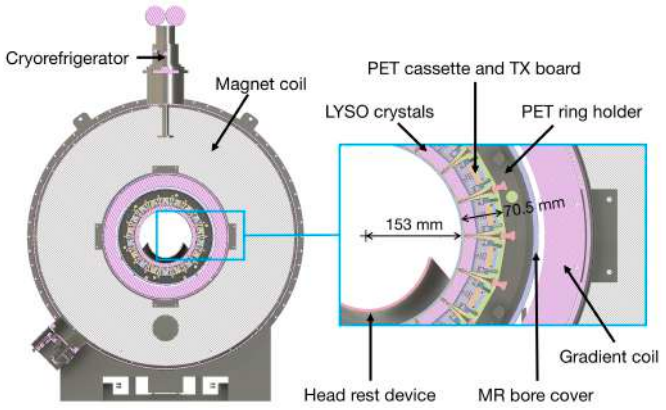

Figure 1. Cross section drawing of the PET/MR system. The RF head coil, not displayed in the figure, is inserted inside the PET bore.

II. Design of the TRIMAGE system

Both MR and PET components have been designed and developed by the TRIMAGE Consortium partners.

A novel type of non-cryogenic (i.e., using no liquid helium or liquid nitrogen) superconducting magnet with a field strength of 1.5 T (SSI, Superconducting Systems, Inc., Billerica, MA 01821, USA) [10] has been used by RS2D (RS2D, Mundolsheim, France) to build the MR component. The magnet coil is cooled with a pulse tube cryorefrigerator (PT410 model by Cryomech, Syracuse, USA). The magnet has a very compact design with an inner diameter of 720 mm and a length of 1300 mm. The compactness of the system and the use of a cryogen-free magnet result in an easier installation and reduced maintenance cost. In fact, the total weight of the TRIMAGE system is about 2300 kg which is half the weight of a clinical 1.5 T MR [11] and no quench pipe is needed in the room, thus simplifying the installation site preparation and safety requirements. Furthermore, the axial length is short enough to leave the patient's arms outside of the magnet thus mitigating the discomfort of claustrophobic patients and giving the possibility of PET bolus injection under control. When equipped with gradient coils, the free bore available for the installation of the PET system has a diameter of 580 mm (Figure 1).

The PET component of the TRIMAGE system is designed to feature better performance than clinical PET/MR systems. Design specifications for spatial resolution and maximum sensitivity at the center of the field of view are <2.5 mm FWHM and 6%, respectively. These values are significantly better than a state of the art clinical systems such as the GE SIGNA PET/MR that has a spatial resolution of about 4.0 mm at the center of the field of view and a maximum sensitivity of 2.3% [6]. The TRIMAGE PET is made of a full ring of 18 sectors in the form of rectangular detectors, 55 mm (transversal) × 163 mm (axial) size. The number and size of sectors is chosen as a compromise between FOV extension (enough for accommodating a RF head coil inside it) and compactness (for fitting into the MR system). Each PET cassette is 70.5 mm thick and the ring outer diameter of 452 mm.

The design of the PET acquisition system includes a series of choices made for MRI compatibility. The standard metallic parts and electronic components are replaced with non-magnetic alternatives whenever possible. All the PET electronics are in RF-shielded enclosures. In particular the RF-shielding of the detectors has been specifically designed to optimize the suppression of PET electronics RF emissions and to be transparent to the gradient fields [12]. In order to minimize any influence of the MR magnetic fields to the analog photodetector outputs, PET data digitization happens in proximity of the SiPMs inside the detectors as in [13] and [14]. This is achieved by placing the ASICs close to the SiPMs and embedding an FPGA in each detector and implementing most of the event characterization algorithms inside this FPGA. In this way, most of the information is compressed inside the PET detectors thus making the physical connections to the DAQ back-end less demanding. We refer to this approach as "early-digitization". The challenge of early digitization is to fit all the processing electronics and the calibration data inside the FPGA at the front-end of the DAQ system. Data processing is distributed and parallelized thus increasing the overall processing power and scalability of the DAQ system. This is obtained in exchange for a more complex power distribution and dissipation design.

The power supply network of the PET has been custom designed for MRI compatibility. The following solutions have been adopted for this purpose: 1) all the detectors are powered with low voltages in order to avoid switching DC/DC converters inside the magnet bore; 2) the PET power supply is located outside the magnet bore and it has been designed with remote voltage sensing to allow to compensate voltage drops due high current loads; 3) all the power and ground rails follow a star-like pattern in order to avoid loops which the gradient system could couple with. This approach is followed also in the routing of PCB layers inside the PET detectors.

The PET acquired data is finally transferred to the operator console outside the shielded room through optical fibers.

The ring is permanently attached to the MR system through a vibration absorbing support. The inner diameter of the PET ring (including bore cover) is 306 mm, thus leaving enough space for the insertion of the RF head coil that is attached to the PET structure (Figure 1). The head coil is designed to fit the PET bore and to be mechanically compatible with a commercially-available, MR-compatible EEG system (Brain Products, Gilching, Germany). The coil has an elliptical shape so as to lay as close as possible to the patient head with an internal size of 260 mm and 230 mm for the longest and shortest axis, respectively. The coil is also equipped with an integrated RF shield. With this configuration, the patient's head is positioned inside the coil through a sliding bed. When locked in its stop position, the brain is located inside the PET/MR field-of-view (FOV) thanks to a dedicated head rest device that is attached to the patient's bed.

The FOV of the combined PET/MR/EEG system has an inner diameter of 260 mm and an axial extension of 160 mm. By integrating the three relevant modalities, the TRIMAGE

TABLE I
SPECIFICATIONS OF THE PET COMPONENT OF THE TRIMAGE SCANNER

Detector tile	
Crystal material	LYSO:Ce
Crystal pixel size (top/bottom layers)	3.3 mm × 3.3 mm × 8/12 mm
Crystal pixel pitch	3.4 mm
No. of crystals (top/bottom layers)	49/64
System	
No. of sectors	18
No. of modules	54 (18 × 3)
No. of tiles/ASICs	216 (18 × 12)
No. of crystals	24408
Distance between opposing crystals	312 mm
Bore diameter	306 mm
Axial FOV	164 mm
Transaxial FOV	260 mm
Coincidence scheme	1 vs 9

system will facilitate multiparametric characterization of brain tissue in a single diagnostic session [8].

The TRIMAGE project has a primary focus on the study of schizophrenia [15] but the developed scanner can be used for other brain studies including, but not limited to: brain cancer, Alzheimer and dementia.

The aim of the paper is to describe in full detail the final version of the PET detectors and related electronics and to report on their preliminary performance in terms of pixel identification, energy resolution and coincidence time resolution (CTR). The detector calibration procedures are also described. The measurements here described were performed in order to find the optimal working parameters and to validate the adopted solutions and the practical implementation before assembling the whole set of PET sectors and data acquisition electronics.

III. MATERIALS

A. The TRIMAGE PET detectors

Each PET sector consists of three square detector modules hosted in a RF shielded cassette [12]. Each module is divided into four sub-modules, which we refer to as tiles (Figure *2*, left). The full PET ring comprises a total of 216 tiles. Each tile features two segmented LYSO:Ce crystal layers. The top layer (the nearest to the center of the field of view) consists of 7 × 7 crystals of 3.3 × 3.3 × 8 mm3, while the bottom layer has 8 × 8 crystals of 3.3 × 3.3 × 12 mm3. A summary of the specifications of the PET component of the TRIMAGE system are listed in Table I. A black thin separator is placed between adjacent bottom layers to reduce the optical crosstalk between tiles. An enhanced specular reflector (3MTM ESR) is placed on the lateral sides of each crystal. Both layers have a pitch of 3.4 mm and are half-pitch "staggered", i.e., each crystal of the top layer is coupled to four crystals of the bottom layer [16], [17]. This configuration allows performing a dichotomic depth of interaction reconstruction, as photons interacting in different layers are expected to produce different light patterns on the SiPMs [18]. The staggered configuration was chosen in order to reduce the depth of interaction uncertainty and to provide a finer sampling of the lines of response with respect to a single layer with the same pixel pitch [19]. The free half-entry face of the crystals on the borders of the bottom matrix is covered with a reflective adhesive tape.

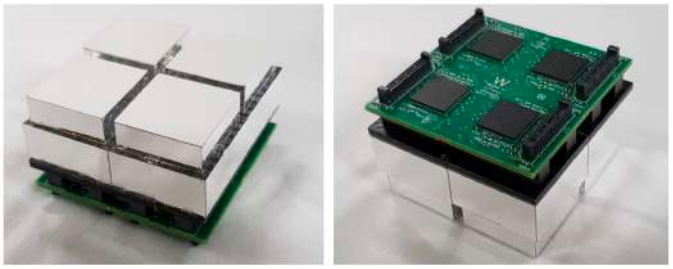

Figure 2. Picture of a TRIMAGE PET detector module. Left: front view showing the four dual-layer tiles. Right: back view showing the ASIC board hosting four TRIROC ASICs.

The crystals in the bottom layer are coupled one-to-one to 64 SiPMs that are arranged in two matrices, specifically designed and manufactured by Advansid s.r.l., Trento, Italy. The model used is an extended version of the hybrid array ASD-NUV3S-P-4x4TD model [20] with of 4 × 8 SiPMs instead of 4 × 4 as in the commercial product. Each SiPM of the array is a NUV type [21], meaning that they have a higher efficiency in the near ultraviolet range (peak efficiency at 420 nm, with detection spectrum extending from 350 nm to 900 nm) that well matches the LYSO emission spectrum. Each element has a size of 3 × 3 mm^2 and a pitch of 3.4 mm, which is modified from the original 3.2 mm of the commercial version so as to match the scintillator pitch. All the 32 SiPMs are mounted on a common package which is completely covered with transparent epoxy layer. A common voltage is used for biasing the whole array through front contacts (i.e., the anode for NUV-SiPMs). Each SiPM is read out individually from the back of the die (i.e., the cathode for NUV-SiPMs), where all the contacts are accessible through an MR-compatible connector. The connector is an application specific model manufactured for this project by Samtec Inc. (New Albany, USA) and features nickel-phosphorus (Ni-Phos) layer plating. The advantage of this solution is that, differently from pure nickel (ferromagnetic), Ni-Phos layers are diamagnetic, thus not interfering with the static B0 field. Each SiPM has 5520 micro-cells, 40 μm side with a 60% fill-factor. The used SiPMs are characterized by a low dark count rate (DCR) and good photon detection efficiency (PDE). At the maximum overvoltage, i.e., 6 V over the breakdown voltage, the manufacturer declares a DCR lower than 100 kHz/mm^2 and a PDE of 43% at 420 nm [20].

A liquid cooling system is used to stabilize the temperature of components located inside the detector cassette (Figure 3). Cold water is distributed with a water chiller and circulated inside each cassette with closed water loops (one every two cassettes). The temperature of the water is 18°C so as to avoid any condensation. The pipe inside the cassette is made of copper. Custom designed cooling blocks made of graphite are used to remove the heat from ASICs, DC/DC converters and LVDS transceivers while a copper block is used for the FPGA. To avoid eddy currents, the copper block is split into two parts and the graphite block is electrically insulated from the pipe.

As of today, all sectors have been fully assembled and two of them were used to perform the measurements described in the present paper.

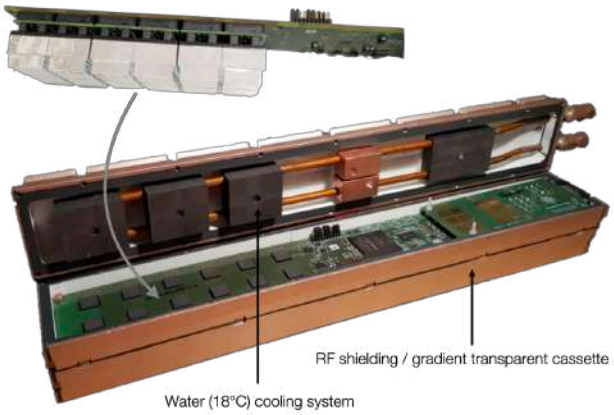

Figure 3. The TRIMAGE PET sector prototype. Top: picture of the three modules attached to the front part of the TX board. Bottom: picture of the same TX board hosted in a RF-shielded cassette. Twelve square holes in the TX board are used to create a thermal contact between cooling blocks (that are attached to the cassette cover) and the ASICs that are located right below the holes and that are also thermally connected to graphite blocks. SiPM temperature is about 26°C.

B. Data Acquisition System and Power Supply

The 64 signals from a tile are read out by a 64-channel TRIROC ASIC [22]. In each analog channel of the ASIC, the input signal is split into a high-gain and a low-gain path for time and charge A/D conversion, respectively. In our implementation, when at least one SiPM output overcomes a programmable threshold along the low-gain path, all SiPM generating a signal above another programmable threshold along the high-gain path are "validated" and acquired as described in [23]. The threshold on the high-gain path is referred to as the time threshold; the threshold on the low-gain path is referred to as the validation threshold, since it validates the former one. Both thresholds are set to the lowest possible value that still allows the rejection of the baseline noise as described in [23].

Four TRIROC ASICs are hosted on a front-end board which we refer to as *ASIC board*. The ASIC board is able to read out all the 256 output signals from a *module* (Figure 2, right). A total of 54 ASIC boards forms the complete PET front-end data acquisition system.

The digital part of the TRIROC ASIC manages the conversion and the data transmission to an FPGA-based board. We refer to this board as the *TX board* as it transmits the acquired data to the back-end for coincidence processing. The ASIC dead time is about 17.2 µs corresponding to a maximum output rate of 58k events per second [23]. The TX board is capable of managing the signals from the 3 ASIC boards (12 ASICs) and is placed in the PET cassette (Figure 3). The FPGA hosted by the TX board is a Cyclone V 5CEFA7F31C6N (Altera Corp., San Jose, USA). A total of 18 TX boards (one per sector) are used in the TRIMAGE PET system.

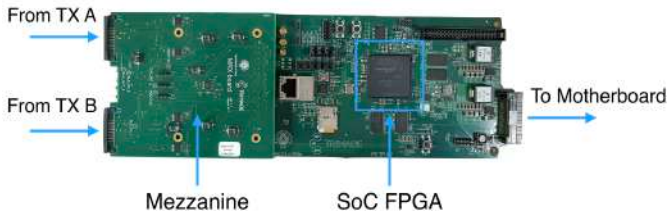

Figure 4. Picture of the RX board showing the on-board SoC FPGA, the mezzanine board (MTX) and the connections to the motherboard and to the two TX boards (named A and B) that are managed by a single RX board.

Every time a TRIROC detects an event, it produces a series of data packets containing the ADC and TDC outputs, one per validated channel [22], [23]. Each data packet is decoded by the FPGA and its TDC payload is calibrated using a calibration map that is loaded on-chip at boot time. For this purpose, we use a quantile-wise time calibration [24], [25]. All the data packets of a single event are referred to as a frame and are stored in the FPGA for on-line processing.

Each frame is elaborated to retrieve the interaction position, the scintillating crystal, the time-stamp of the event as a whole and the total energy (calibrated in keV as described in detail in Section IV.B) released in the interaction. Single events that do not fall within a programmable energy window are discarded. Data can be downloaded from the TX boards either in its final calibrated format, or bypassing all the calibrations. In the former case, the event is encoded in a fixed-length packet of 12 bytes. The latter case is useful only for optimization and debug purposes, since it does not allow to acquire events at the full rate of the ASICs. The TX board also executes a monitoring of the event rate and transmits it periodically to the backend.

The backend system is composed of a motherboard and 9 receiver boards (called RX boards*). Each RX board receives data from two TX boards (*

Figure 4).

The TX boards communicate with the RX boards through two different links: a serial transmission for the slow control commands (such as the transmission of the ASIC settings and the read-out of the registers) and a fast LVDS connection for the data transmission. The TX-FPGA is also implementing a data buffer, in such a way that all data can be transmitted without any loss and with no additional dead time.

The connection between the RX board and the two TX boards is mediated by two mezzanine boards (called *MRX* and *MTX*, respectively) that host LVDS transceivers. The MRX and the MTX are connected through a Samtec HQDP-020-120.0-TED-TEU-1B high-speed shielded differential cable. The cable shielding is attached, at one side only, to the RF-shielding of the cassette.

The RX board acts as a multiplexing interface for the high-speed LVDS data channels between the TX boards and the motherboard. The FPGA used in the RX board is a Cyclone V 5CSXFC6D6F31C7N SoC FPGA (Altera Corp.). The RX board has an independent Ethernet that allows to stream single events data in order to perform coincidence processing offline for research purposes.

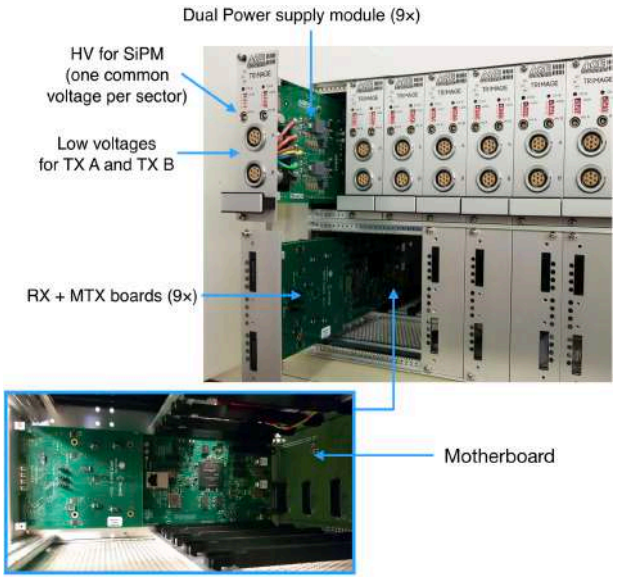

Figure 5. Picture of the 19" shielded cabinet hosting the DAQ and power supply systems. Inside the rack are installed 9 dual power supply modules providing low voltages for the TX boards and the SiPMs bias voltage. The cabinet also contains the 9 receiver boards that are plugged on a motherboard.

The motherboard is based on a Cyclone V 5CGXFC7D6F31C6N FPGA (Altera Corp.). The FPGA multiplexes the data coming from the RX boards, it handles the slow control and sorts all the single events by timestamp. Sorted events are then processed in real time for coincidence detection by timestamp comparison. Only coincidences occurring between a sector and one of the opposing nine sectors are accepted. The motherboard is connected to a local host PC through a USB 2.0 connection allowing a maximum data transfer rate of about 40 MB/s. Considering a packet of 24 bytes for each coincidence event, this limit corresponds to a maximum coincidence count rate of about 1.5 Mcps.

The FPGA on the motherboard collects also several counting statistics, e.g., event losses due to the saturation of the USB connection, singles count rates and random coincidence rates. Random coincidence rates are determined with the delayed window technique, i.e., by comparing the timestamps of the events stream with a time-shifted copy of the same stream. A common 160 MHz LVDS clock is generated in the motherboard and distributed to the RX boards which forward it to all the TX boards via the data cable. A pictorial scheme of the data acquisition chain can be found in [23].

A custom power supply has been developed for remotely biasing the SiPMs (30 ± 3 V range, 10 mA maximum current) and suppling the low voltages required by the TX FPGAs and the ASICs, i.e., 1.5 V (12 A maximum current) and 3.3 V (10 A). Each low voltage power rail is provided with a feedback line that is used to compensate any voltage drop through the power cables. The power supply provides one common SiPM bias voltage for each sector, which can be then adjusted on a per-channel basis by the ASICs. The maximum applicable adjustment is -2 V. A host board (backplane) can support up to

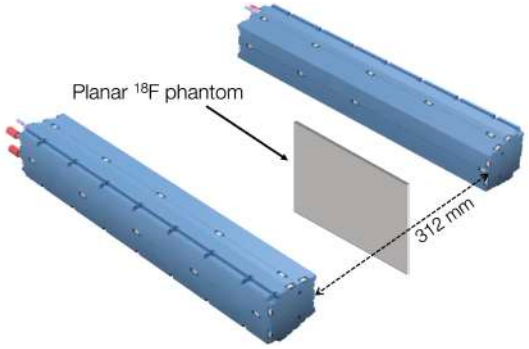

Figure 6. Drawing of the testing setup for pixel identification, energy and CTR measurements. The supporting ring is not displayed in the figure.

9 power modules, each providing the required power rails for two TX boards. The maximum total power of each module is 40 W. The power supply system comes in a standard 19" rack box with removable cassettes, one every two power modules. Each channel is controlled by the DAQ PC through the backplane with a serial interface. The power modules are designed to have their output voltage disabled at startup and in case of overload for safety reasons. Their microcontroller will then retrieve the operating values from a non-volatile memory on-board. The remaining low voltages (1.1 V and 2.5 V) that are needed by the TX board are generated by low-dropout (LDO) DC linear voltage regulators hosted on the MTX boards. The total power consumption of a PET sector is about 15 W. A 12 V primary supply positioned outside the MR room provides power through the MR-room filter plate to the DAQ cabinet, which is inside the MR room. The DAQ cabinet includes: 1) the motherboard: 2) the DAQ PC; 3) the remote power supply for the TX boards and SiPMs and 4) the ethernet-to-fiber adapter that connects the DAQ PC to the client PC outside the MR room (

Figure 5).

IV. Methods

A. Testing setup

For pixel identification, energy and CTR measurements a planar phantom (150 mm long × 60 mm high × 2 mm thick + 2 mm PMMA walls) filled with a ^{18}F source with an activity of 8 MBq was placed in the mid plane between the two sectors which are located in opposing positions in the ring (

Figure 6). The position and size of the phantom allows filling all the possible lines of response thus obtaining a flood field irradiation.

In order to find the optimal SiPM bias voltage, measurements were performed at different voltages, from -29.5 V to -32.1 V, with a step of 0.2 V. For the sake of simplicity, when referring to higher or lower bias voltages, we are considering the absolute value. For these measurements, all SiPMs in a sector are biased at the same voltage. Although the ASIC offers the possibility to adjust the bias of each SiPM, in this study, the bias voltage adjustment is shared among all the channels of a tile, while

channel-wise adjustment is left as a future work.

During the data taking, with the cooling system in use, the temperature of the SiPMs was measured with a temperature transducer and resulted constant at 26 °C.

B. Flood maps, LUT generation and energy calibration

The calibration of each tile consists of four steps: flood map generation, pixel centers identification, generation of crystal look-up table and energy calibration.

Flood maps were generated by calculating the 2D histogram of the center of gravity (COG) of each reconstructed frame. In fact, even if there is a one-to-one coupling between crystal pixels and SiPMs for the bottom layer, the identification of top layer pixels requires the information from more than one SiPM channel. The coordinates of the centers are evaluated as in [23], i.e.:

$$x = \frac{\sum_{i=1}^{8} i \cdot x_i}{E};\ y = \frac{\sum_{i=1}^{8} i \cdot y_i}{E};\ E = \sum_{i=1}^{8} x_i \qquad \text{Eq. 1}$$

Where x_i (y_i) are the sums of all the signals collected by the the i^{th} SiPM row (column) after having subtracted the measured baseline from each signal. Although other methods have been explored with potentially better performance in terms of pixel identification, such as Support Vector Machine techniques [6], the COG calculation was chosen because if its simplicity and ease of implementation in the FPGA. When generating the flood maps and energy spectra, we do not apply any energy filter and we use a coincidence window of 3 ns.

An automatic calibration software identifies the crystal centers, using the multiscale dot enhancer filter described in [26]. The pixel identification look-up-tables (LUT) are then built using the centers found in the previous step as seeds for a Voronoi partitioning [27]. Using the LUT, events are then attributed to a pixel/layer.

In order to select the bias voltage that provides the best compromise between the quality of pixel identification in both layers, we have evaluated the Resolvability Index (RI) [28], averaged among pixels belonging to the same layer, as the figure of merit for flood map comparison. The RI is defined as the ratio between the FWHM of crystal spots in flood histogram and the average distance between the spot and its neighbors. The use of the RI is recognized to be more adequate than the peak-to-valley ratio for that purpose when peaks are very well resolved [29].

The raw energy of an event is obtained from the sum of the signals detected by all the validated SiPMs. Once the raw energy histogram of each pixel is computed, it is possible to equalize the gain of each channel and to calibrate it in keV using the full energy peak as the reference for the 511 keV. Energy spectra for the bottom and top layers are then obtained by aligning all spectra to 511 keV and summing up all the events assigned to the same layer. No correction for the saturation of the SiPM is applied.

Another important parameter to consider for bias voltage setting is the counting efficiency of both layers. Using the same acquisitions performed for flood map evaluation, we evaluated the average number of counts per pixel, defined as the absolute number of counts recorded in the energy window between 350 keV and 650 keV in each layer divided by the number of pixels in the same layer. Measured counts were then corrected for the decay of the ^{18}F source to make the various measurements comparable with the others. Dead time correction was negligible in all measurements. Crystals at the border of the bottom layer were not considered because, for being not fully shielded by the top layer, they have a higher efficiency than the inner crystals.

The energy resolution of the detectors (reported in percent) was evaluated as the average value of the full width at half maximum of the full energy peak of each layer of a tile divided by 511 keV.

C. Count rate and CTR measurement

In order to confirm that the TX board is capable of transmitting data to the backend at the maximum count rate allowed by the ASICs, data were acquired using the planar source filled with a ^{18}F solution. Nine acquisitions were performed at regular time intervals over 8 hours starting with an initial activity that was able to saturate the maximum count rate.

The CTR has been first evaluated for a pair of tiles only, in order to evaluate the variation against the bias voltage. In this case, both tiles where biased at the same voltage. Once the optimal bias voltage was found and set for all tiles, the CTR was measured for a pair of sectors. Separate CTR values for the top (top-to-top layer coincidences, only) and bottom layer (bottom-to-bottom layer coincidences, only) have been calculated. The stability of the CTR of a pair of sectors against the count rate was also studied. For this measurement, a common bias voltage of -30.7 V was applied to all tiles.

In all cases, data were filtered with a 3 ns wide coincidence window and with an energy window between 350 keV and 650 keV. The timestamp assigned to each event was calculated from the energy-weighted average of the timestamps of all the channels triggered by the event. The energy-dependent time walk effect has also been corrected. This effect consists in the fact that a higher energy event signal has a sharper edge and crosses the timestamping threshold earlier than a lower energy one, thus leading to an energy dependent bias in the estimation of its time of arrival. This bias has been calculated (and subtracted) fitting the difference in time of arrival as a function of the difference in energy between coincident events [30].

V. Results

A. Pixel identification

We have obtained the flood maps of each of the 24 tiles for different SiPM bias voltages. All tiles have the same behavior against the bias voltage. Sample flood maps of a tile biased at four different voltages are shown in

Figure 7. In each image, the minimum value displayed is zero (white) while the maximum is set as the highest value (black) in the map excluding the outer pixels. This rescaling was necessary because the outer (and corner in particular) pixel peaks are much higher than the others making them hard to be

displayed. Only four voltages (-29.5 V, -30.3 V, -31.1 V and -31.9 V) are here reported for simplicity.

At a first visual inspection, one can observe that at lower voltages, only the bottom layer is well visible, while the at higher voltages both layers start to be blurred.

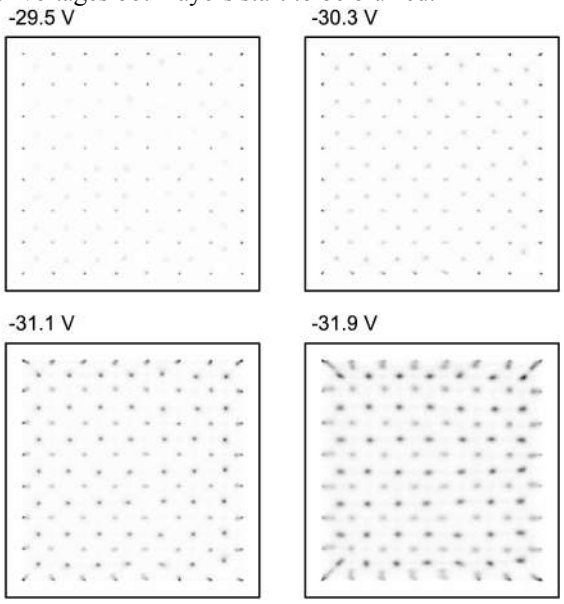

Figure 7. Flood maps of a single tile biased at different bias voltages. In each image, white is zero, while black corresponds to the highest value in the map excluding the outer pixels.

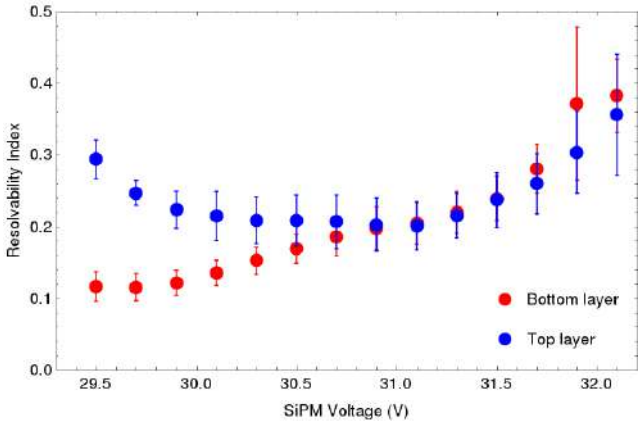

Figure 8: Pixel identification expressed as the average RI of pixel spots in the top (blue dots) and bottom (red dots) layers.

Figure 8 shows the RI of pixels in the top and bottom layers for the same tile used to show the flood map. Even if the RI cannot be considered as a measure of the crystal identification power or detector spatial resolution, it can still be used as one of the important parameters to be evaluated for the choice of the optimal bias voltage for each tile. In Figure 8, we can identify a range of bias voltages, i.e., from -29.9 V to -31.5 V where spots in the flood map are very well separated (RI<0.25). This can be clearly seen in Figure 9 where the peak profile obtained along the diagonal direction (from bottom left to top right) of the same tile, biased at -31.1 V, is displayed.

B. Energy resolution and efficiency of layers

An example of the energy spectra of the top and bottom layers of a single tile is shown in Figure 10. The applied bias voltage was -31.1 V. The energy resolution at 511 keV is 22% for the top layer and 20% for the bottom one.

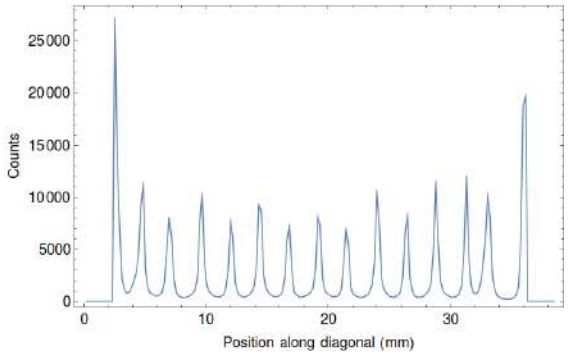

Figure 9. Profile of the flood map measured at -31.1 V obtained along the diagonal direction, from bottom left to top right. The odd number peaks (1st, 3rd, ...) are relative to the bottom layer while the even ones (2nd,4th, ...) belongs to the top layer. Peak profiles of corner pixels (the first and the last) are higher than other bottom layer pixel profiles for the better FWHM and because they are shielded by the top layer by one quarter of the size only, while inner pixels are fully shielded. Excluding corner pixels, peak profiles of top layer pixels are higher than the bottom layer. Considering an equal RI for the two layers, the relative peak height suggests that the top layer has a higher efficiency of the bottom one.

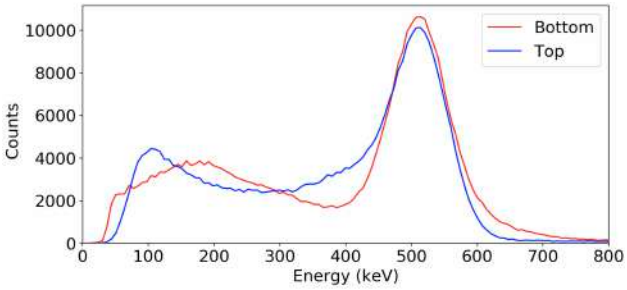

Figure 10. Energy spectra (-31.1 V bias voltage) for a top (blue) and bottom (red) layers. No energy cut was applied to the spectra.

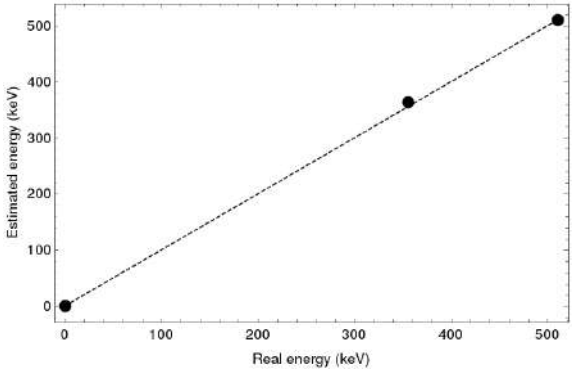

Figure 11. Plot the energy spectra linearity check using the 356 keV line of a ^{133}Ba source. The 0 keV and 511 keV data points have been used for energy calibration, which is represented by the dashed line joining them.

The linearity of the energy plot was verified using the 356 keV line of a ^{133}Ba source (Figure 11). The measured energy of the ^{133}Ba peak is 361 keV, in good agreement with its actual value; this shows that there is no significant loss of linearity up to 511 keV.

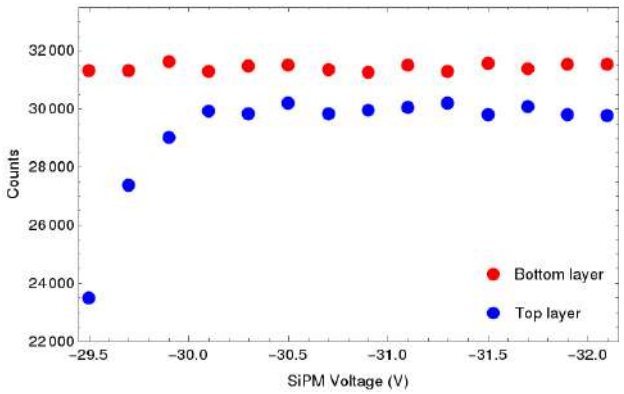

Figure 12: Plot of the average number of counts identified in crystals of the top (blue dots) and bottom (red dots) layers. The energy window is 350-650 keV. Crystals at the border of the bottom layer were not considered.

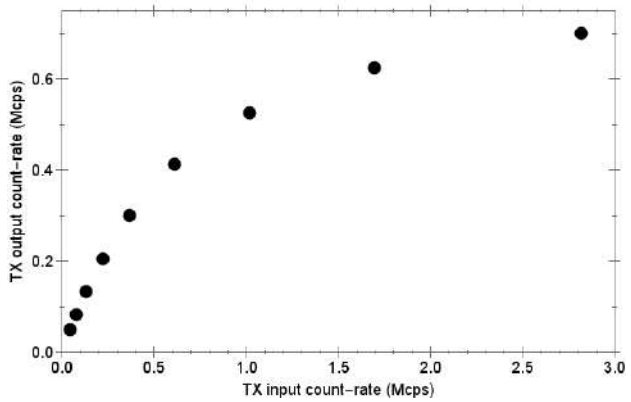

Figure 13: Plot of the single event count rate of a PET sector against the input count rate.

Figure 12 shows the result of the evaluation of the counting efficiency of the two layers of a tile. After the application of the energy window, the bottom layer has more counts per pixel than the top layer, thus inverting the situation observed in Figure 9.

The efficiency of the bottom layer remains constant over the whole range of bias voltages while the top layer shows a reduction in efficiency below -30.3 V, confirming the effect observed in the flood map for lower voltages. This value should be then considered as the lowest possible bias voltage for this specific tile. This procedure was repeated for all tiles, then identifying the working range of bias voltages for each of them.

C. Count rate and CTR

Figure 13 shows the single event count rate transmitted from the TX board and acquired by the back-end DAQ as a function of the input count rate, i.e., the number of counts that would have been recorded with a zero dead time. The input count rate is derived by extrapolating the counts with a linear fit using the first three points in the plot, assuming a negligible contribution of dead time at low count rates. The plot follows the expected behavior for twelve independent detectors with a non-paralyzable dead time of about 17.2 μs [23]. The observed maximum count rate is about 700 kcps, which is approximately twelve times the maximum count rate allowed by one ASIC.

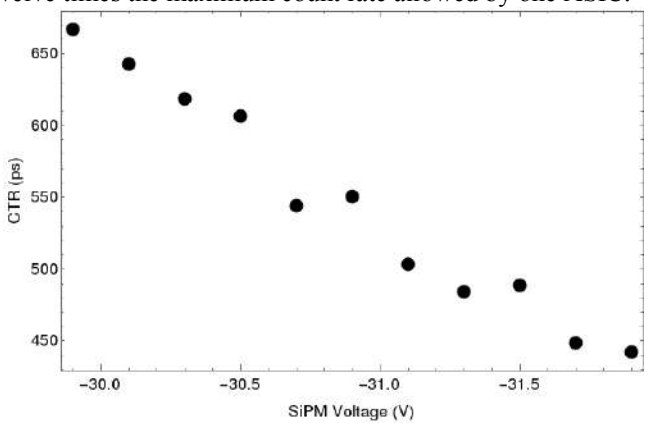

Figure 14: Plot of the CTR of a pair of tiles against the bias voltage applied to both tiles.

TABLE II
OPTIMAL BIAS VOLTAGES FOR THE 24 CONSIDERED TILES

Sector 1				
Module n.	ASIC 1	ASIC 2	ASIC 3	ASIC 4
1	-31.1 V	-31.1 V	-30.9 V	-31.3 V
2	-32.1 V	-31.5 V	-31.5 V	-31.3 V
3	-31.1 V	-30.7 V	-31.1 V	-29.9 V
Sector 2				
Module n.	ASIC 1	ASIC 2	ASIC 3	ASIC 4
1	-31.5 V	-31.1 V	-29.7 V	-31.1 V
2	-31.1 V	-29.9 V	-30.9 V	-31.5 V
3	-31.9 V	-31.3 V	-31.5 V	-31.1 V

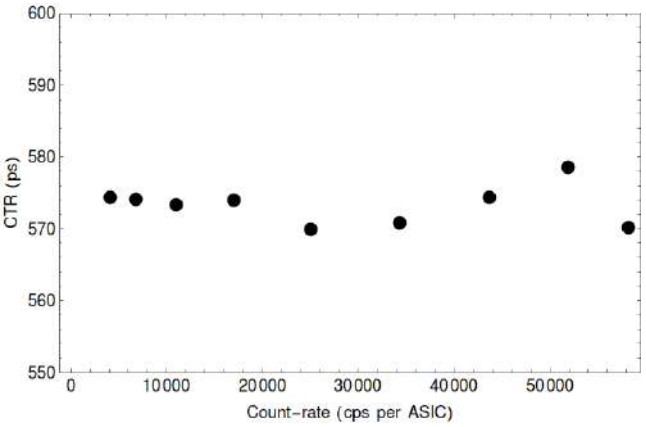

Figure 15: CRT of a pair of tiles measured at different count rates. Both tiles were biased to – 30.7 V.

This observation confirms that the data stream from the twelve ASICs of a PET sector to the backend does not suffer from any significant losses. Considering 12 bytes per single event, the maximum data rate expected from the TX board to the RX board is 8.4 MB/s, well below the maximum bandwidth of the LVDS interface (200 MB/s). Thanks to the early

digitization occurring in the TX-FPGA, the maximum count rate is not affected by the number of SiPM channels activated in each event.

Figure 14 reports the results of the CTR of a pair of tiles as a function of the bias voltage. The CTR improves with increasing the bias voltage for the linear increase of the SiPM PDE with the bias voltage [20]. These results suggest to use the highest among the possible values of bias voltage so as to obtain the best results in terms of CTR.

For the tile analyzed in this paper, we have selected -31.1 V as the optimal bias voltage. Higher voltages are also possible, even if some saturation of the ASIC preamplifiers can be observed especially at the outputs of the SiPMs coupled to the crystals at the borders of the tile.

The procedure was repeated for all tiles in the two considered sectors obtaining the optimal bias voltage for each tile. The results of the optimization procedure are reported in Table II.

The measured CTR measured for a pair of sectors, where all the tiles were regulated individually to the optimal bias voltage value, is 515 ps. The CTR was also evaluated separately for the two layers. Measured values were 529 ps for the top layer and 501 ps for the bottom layer. The value of the CTR, measured between two tiles, does not show any particular trend as a function of the count rate (see **Error! Reference source not found.**), even if the measurement seems to become more unstable as the count rate approaches the saturation value.

VI. Discussion

The design choice of the dual layer configuration with staggered crystal matrices has the potential advantage of reducing the parallax effect while also offering an oversampling of the lines of responses. A possible drawback of this approach is the higher dynamic range required by the SiPM and the relative readout electronics. This is especially true for the one-to-one coupling of crystals to SiPM that we have in the bottom layer. In fact, in our configuration, pixels in the bottom layers release most of the emitted light in one pixel only, while top layer pixels share it among four SiPMs. This consideration suggests that the optimization of the SiPM bias voltage is critical for working in a condition where detector performance is not compromised.

In this study we have observed that when the SiPM bias voltage is set in the working range, all top layer events that have an energy above the threshold along the low-gain path of the ASIC, have at least four SiPM channels validated and recorded. However, when the bias voltage is too low, we start recording events with less than four validated channels. This effect results in an increase of the RI and a loss of efficiency in the top layer. The lost data correspond to interactions where none of the four SiPMs signals is strong enough to overcome the ASIC threshold. On the other hand, when an excessive bias voltage is applied, interactions occurring in one pixel of the bottom layer may produce a signal saturation in the ASIC channel corresponding to the SiPMs coupled to it, while neighboring channels start to pass the validation threshold. These two effects make the set of recorded channels more unstable and, when used for the COG calculation, the result is an increase in pixel blurring.

The bias voltage optimization procedure implemented in this work has demonstrated to be applicable to all tiles with a maximum observed variability of 2.2 V. Most of this difference can be compensated by the bias voltage adjustment offered by the ASIC. Any residual difference of few tenths of volt can be neglected because, according to the results reported in Figure 8 and Figure 12, no significant variation in resolvability index and detection efficiency is observed for small variations of the bias voltage.

The worse energy resolution of the top layer can be attributed to the higher light dispersion occurring when most of the scintillation light is shared among four pixels. However, the difference is quite small (about 2%) because, also in the case of bottom layer interactions, there is some light sharing to the neighbor SiPMs. Probably, this effect is mainly caused by the scintillation light that, travelling in the direction opposite to the SiPM, enters in the four corresponding crystals of the top layer and then it is reflected back to the bottom layer. The obtained energy resolution is still comparable with similar systems [2], [4] while better performances (~13%) were obtained by other brain PET/MR scanners featuring single layer matrices [3] or monolithic blocks [5].

The one-to-one coupling of SiPMs to the bottom layer, that concentrates most of the scintillation light on few SiPMs, and the possibility to process all SiPM outputs contribute to the achievement of a CTR of 515 ps. Although still not better than the timing performance offered by most recent whole body TOF-PET systems, the TRIMAGE PET detectors outperforms, to our knowledge, all the other dedicated brain PET/MR detectors. Even if not aiming to TOF-PET applications, this value still contributes to the reduction of the random count rate. The CTR is also compatible with the best CTR (420 ± 20 ps) we have achieved with two crystal pixels only [23]. This difference can be justified with the increased light dispersion due to the staggered configuration.

The choice of a one-to-one coupling of SiPMs to bottom layer pixels and the possibility to readout all the SiPM signals allows a robust pixel identification in both layers with a RI<0.2 obtained using the COG calculation. In addition, it would also open the possibility to perform additional data processing, such as the implementation of different and more complex algorithms for pixel identification or for the classification inter crystal scatter events [18] directly within the front-end FPGA, that can hardly be possible using the multiplexing readout schemes implemented in other brain PET/MR systems.

VII. Conclusions

We have presented the design and the preliminary performance of the detectors and the data acquisition system of the PET component of the TRIMAGE brain trimodality PET/MR/EEG scanner. We have defined the procedure for optimizing the bias voltage of each SiPM tile and preliminary tests on the first two PET sectors operated in the final configuration where performed. All pixels can be identified with a RI of about 0.2, indicating a negligible contribution of pixel identification to the system spatial resolution. The maximum singles count rate of a PET sector is about 700 kcps.

The energy resolution of a single tile is 20% FWHM and 22% FWHM for the bottom and top layer, respectively, while the CTR of two detectors is 515 ps.

These results were obtained using the final data acquisition electronics, confirming the results of the early detector characterization done with a prototype system [23]. The data acquisition frontend showed a maximum singles count rate capability of 700 kcps for each of the 18 sectors, while the acquisition of coincidence events is limited to a maximum of 1.5 Mcps by the USB 2.0 connection at the backend. These numbers apper to be balanced, but the way they affect the maximum injectable activity depends on the radioisotope distribution in the body that is strongly related on the used radiotracer. A full understanding of this aspect will be studied when the full PET systems is assembled and tested on patients.

Future work will be devoted to the assembling and optimization of the whole PET ring and to the evaluation of the MR compatibility of the system that can be fully verified only once the system will be fully integrated in the MR component.

REFERENCES

[1] A. Kolb *et al.*, "Technical performance evaluation of a human brain PET/MRI system," *European Radiology*, vol. 22, no. 8, pp. 1776–1788, Aug. 2012.

[2] J. H. Jung *et al.*, "Development of PET/MRI with insertable PET for simultaneous PET and MR imaging of human brain," *Medical Physics*, vol. 42, no. 5, pp. 2354–2363, Apr. 2015.

[3] P. Olcott *et al.*, "Prototype positron emission tomography insert with electro-optical signal transmission for simultaneous operation with MRI," *Physics in Medicine and Biology*, vol. 60, no. 9, pp. 3459–3478, May 2015.

[4] F. Nishikido *et al.*, "Development of a full-ring 'add-on PET' prototype: A head coil with DOI-PET detectors for integrated PET/MRI," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 863, pp. 55–61, Aug. 2017.

[5] J. M. Benlloch *et al.*, "The MINDVIEW project: First results," *European Psychiatry*, vol. 50, pp. 21–27, Apr. 2018.

[6] A. M. Grant, T. W. Deller, M. M. Khalighi, S. H. Maramraju, G. Delso, and C. S. Levin, "NEMA NU 2-2012 performance studies for the SiPM-based ToF-PET component of the GE SIGNA PET/MR system: PET performance measurements of the GE SIGNA PET/MR," *Medical Physics*, vol. 43, no. 5, pp. 2334–2343, Apr. 2016.

[7] S. Vandenberghe and P. K. Marsden, "PET-MRI: a review of challenges and solutions in the development of integrated multimodality imaging," *Physics in Medicine and Biology*, vol. 60, no. 4, pp. R115–R154, Feb. 2015.

[8] N. J. Shah *et al.*, "Advances in multimodal neuroimaging: Hybrid MR–PET and MR–PET–EEG at 3T and 9.4T," *Journal of Magnetic Resonance*, vol. 229, pp. 101–115, Apr. 2013.

[9] TRIMAGE: A Dedicated Trimodality (PET/MR/EEG) Imaging Tool for Schizophrenia [online], retrieved from: http://www.trimage.eu/, 2018.

[10] Superconducting Systems, Inc. 1.5T, 720mm Magnet for Human MRI [online], retrieved from: http://www.superconductingsystems.com, 2018.

[11] Philips Healthcare, Ingenia 1.5T MR system [online], retrieved from: http://www.usa.philips.com/healthcare/product/HC781341/ingenia-15t-mr-system., 2018.

[12] A. Berneking *et al.*, "Design and Characterization of a Gradient-Transparent RF Copper Shield for PET Detector Modules in Hybrid MR-PET Imaging," *IEEE Transactions on Nuclear Science*, vol. 64, no. 5, pp. 1118–1127, May 2017.

[13] M. Carminati *et al.*, "SPECT/MRI INSERT Compatibility: Assessment, Solutions, and Design Guidelines," *IEEE Transactions on Radiation and Plasma Medical Sciences*, vol. 2, no. 4, pp. 369–379, Jul. 2018.

[14] P. Gebhardt, J. Wehner, B. Weissler, R. Botnar, P. K. Marsden, and V. Schulz, "FPGA-based RF interference reduction techniques for simultaneous PET–MRI," *Physics in Medicine and Biology*, vol. 61, no. 9, pp. 3500–3526, May 2016.

[15] A. Del Guerra *et al.*, "TRIMAGE: A dedicated trimodality (PET/MR/EEG) imaging tool for schizophrenia," *European Psychiatry*, vol. 50, pp. 7–20, Apr. 2018.

[16] Nan Zhang, C. J. Thompson, D. Jolly, F. Cayouette, and S. Kecani, "A prototype modular detector design for high resolution positron emission mammography imaging," in *2002 IEEE Nuclear Science Symposium Conference Record*, Norfolk, VA, USA, 2003, vol. 2, pp. 858–862.

[17] N. Belcari, F. Attanasi, V. Rosso, and A. Del Guerra, "Staggered double-layer array crystals for the reduction of the depth-of-interaction uncertainty in in-beam PET: A preliminary study," *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 617, no. 1–3, pp. 246–247, 2010.

[18] N. Camarlinghi *et al.*, "Evaluation of Algorithms for Photon Depth of Interaction Estimation for the TRIMAGE PET Component," *IEEE Transactions on Nuclear Science*, vol. 63, no. 1, pp. 70–74, 2016.

[19] C. Thompson *et al.*, "Comparison of single and dual layer detector blocks for pre-clinical MRI–PET," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 702, pp. 56–58, Feb. 2013.

[20] Low afterpulse NUV SiPMs ASD-NUV3S-P-4x4TD [online], available at: http://advansid.com/products/product-detail/asd-sipm3s-p-4x4td, 2018.

[21] T. Pro *et al.*, "New Developments of Near-UV SiPMs at FBK," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 2247–2253, Jun. 2013.

[22] S. Ahmad *et al.*, "Triroc: A Multi-Channel SiPM Read-Out ASIC for PET/PET-ToF Application," *IEEE Transactions on Nuclear Science*, vol. 62, no. 3, pp. 664–668, Jun. 2015.

[23] G. Sportelli *et al.*, "The TRIMAGE PET Data Acquisition System: Initial Results," *IEEE Transactions on Radiation and Plasma Medical Sciences*, vol. 1, no. 2, pp. 168–177, Mar. 2017.

[24] Jian Song, Qi An, and Shubin Liu, "A high-resolution time-to-digital converter implemented in field-programmable-gate-arrays," *IEEE Transactions on Nuclear Science*, vol. 53, no. 1, pp. 236–241, Feb. 2006.
[25] P. Carra *et al.*, "Auto-calibrating TDC for a SoC-FPGA data acquisition system," *IEEE Transactions on Radiation and Plasma Medical Sciences*, p. (in press), 2018.
[26] Q. Li, S. Sone, and K. Doi, "Selective enhancement filters for nodules, vessels, and airway walls in two- and three-dimensional CT scans," *Medical Physics*, vol. 30, no. 8, pp. 2040–2051, Jul. 2003.
[27] Q. Du, V. Faber, and M. Gunzburger, "Centroidal Voronoi Tessellations: Applications and Algorithms," *SIAM Review*, vol. 41, no. 4, pp. 637–676, Jan. 1999.
[28] C. J. Thompson and A. L. Goertzen, "Evaluation of a 16:3 Signal Multiplexor to Acquire Signals From a SPM Array With Dual and Single Layer LYSO Crystal Blocks," *IEEE Transactions on Nuclear Science*, vol. 58, no. 5, pp. 2175–2180, Oct. 2011.
[29] A. L. Goertzen *et al.*, "Design and Performance of a Resistor Multiplexing Readout Circuit for a SiPM Detector," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1541–1549, Jun. 2013.
[30] Z. Deng, A. K. Lan, X. Sun, C. Bircher, Y. Liu, and Y. Shao, "Development of an Eight-Channel Time-Based Readout ASIC for PET Applications," *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 3212–3218, Dec. 2011.