

Reliable fabrication of metal contacts on silicon nanowire forests

Elisabetta Dimaggio* and Giovanni Pennelli

Dipartimento di Ingegneria della Informazione, Università di Pisa, Via G.Caruso, I-56122 Pisa, Italy

We present a technique for the fabrication of an electrical (and thermal) contact on the top ends of a large number of vertical silicon nanowires, which are fabricated perpendicularly to a silicon wafer (silicon nanowire forest). The technique is based on electrochemical deposition of copper and it has been developed on silicon nanowire forests, fabricated by metal assisted chemical etching. We demonstrate that copper grows selectively only on the top end of the silicon nanowires, forming a layer onto the top of the forest. The presence of a predeposited metal seed is fundamental for the selective growth, meanwhile the process is very strong with respect to other parameters, such as concentration of the electrolytic solution and current density, used during the metal deposition. Typical $I - V$ characteristics of top-to-bottom conduction through silicon nanowire forests with different n -doping are shown and discussed.

Keywords: nanowire, thermoelectricity, metal assisted chemical etching, electrodeposition

In the last years, silicon nanowires (SiNWs) have been proposed as building blocks for a large variety of applications such as advanced electronic devices[1, 2], sensors with enhanced sensitivity[3, 4], advanced solar cells[5–7], and others. Very recently, it has been demonstrated that thermal conductivity in silicon nanowires is strongly reduced with respect to that of bulk silicon[8, 9]. This thermal conductivity reduction is more effective in rough SiNWs[10, 11] because, as reported by several theoretical works[12, 13], phonon conduction is dominated by the surface scattering. Phonon conductivity suppression is very effective in nanowires narrower than 100 nm, meanwhile electron transport is only slightly affected by surface scattering, unless the nanowire width is below 20 nm. Therefore, there is a large range of nanowire widths for which the ratio between the electrical conductivity σ and the thermal conductivity k_t is very high in comparison with that of bulk silicon. For this reason, silicon nanowires are very promising for the fabrication of thermoelectric generators with high thermal-to-electrical conversion efficiencies.

Devices based on silicon nanowires can be fabricated by means of top-down approaches[14–16]. Alternatively, bottom-up nanowires, grown by means of Vapour-Liquid-

Solid (VLS) epitaxy[17, 18], can be positioned between electrical contacts to achieve functional devices. For sensing and, in particular, thermoelectric applications, a large number of nanowires must be connected together in order to increase both the mechanical strength of the device and the electrical current (hence the power) that the device can deliver. In principle, complex networks of silicon nanowires can be fabricated on large areas[19, 20] by means of top-down approaches based on lithography and etch. Since these approaches are based on advancements of the technologies employed for integrated circuits fabrication, they are very promising in view of a large scale industrial production. However, nanowires are placed in parallel with the substrate, whose thermal conductivity degrades the thermoelectric performances. All the aforementioned application fields would benefit from the use of SiNW placed perpendicularly to the silicon substrate, because a considerably larger number of nanowires, with respect to planar strategies, can be achieved on the same area. In particular, thermoelectric devices based on silicon nanowire forests could deliver high electrical currents, due to the large number of parallel vertical nanowires. These nanowire forests can be massively produced both by bottom-up growth, through catalysing seeds, and by top-down techniques, through anisotropic etching. Even if lithography and highly directional plasma etching can be used for this purpose, inexpensive metal assisted chemical etching (MaCE)[21, 22], which has been considered in this experimental work, allows the fabrication of nanowires smaller than 100 nm in diameter and with a length of several tens of micrometers. Both strategies (bottom up and top down) allow the fabrication of forests made of a large number of vertical nanowires on areas of the order of several centimetres square, as schematically shown in Figure 1.

The key point is to provide a common electrical (and thermal) contact which connects the top ends of the nanowires, meanwhile the substrate, which is made of bulk silicon which has a good thermal and electrical conductivity, provides the common contact at the bottom ends of the nanowires (see Figure 1). Possible techniques for the fabrication of the top contact, consisting in embossing the nanowire forests in polymers, have been

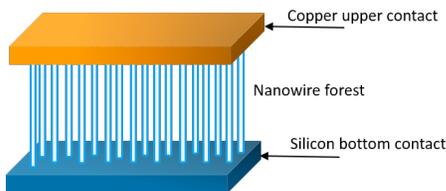


FIG. 1. Sketch of vertical nanowires contacted on the top ends. The silicon substrate, which has a good thermal and electrical conductivity, provides the bottom contact.

* elisabetta.dimaggio@ing.unipi.it, tel. +39 050 2217 672, fax. +39 050 2217522

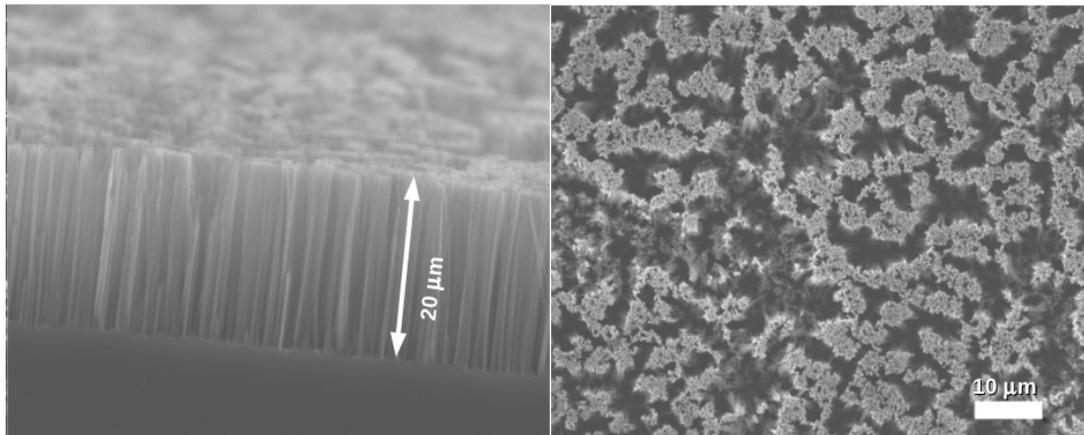


FIG. 2. SEM images of a typical nanowire forest, obtained by etching a Si $\langle 100 \rangle$ substrate (resistivity $\rho = 1 - 10 \Omega\text{cm}$) in $\text{HF} : \text{AgNO}_3 : \text{H}_2\text{O}$ 16:5:60 for 120 min. Left panel: cross section. Right panel: top vision.

proposed[23, 24]. However, nanowire forests embedded in polymers cannot be used for sensing purposes. As far as thermoelectric applications are concerned, the temperature range is limited by the presence of polymer, and moreover the polymer thermal conductivity decreases the conversion efficiency.

We present a possible technique for the fabrication of the top contact based on the selective growth of copper, by electrodeposition, on the top ends of the nanowires: in section I the main points of the process are shown and discussed. In section II, we show that the process is very robust with respect to the current density and solution conditions. In section III, $I-V$ characteristics of devices, based on nanowire forests with different doping concentrations, are shown and discussed.

I. COPPER ELECTRO-DEPOSITION ON NANOWIRE FORESTS

Vertical silicon nanowires, narrower than 100 nm in diameter, have been fabricated by means of Metal assisted Chemical Etching (MaCE). This simple and cheap top-down technique, largely investigated in the last years[21], is based on the selective HF etching of silicon which is locally oxidized by an agent through the catalysis induced by metal nanoparticles. MaCE allows the simultaneous fabrication of a large number (more than 10^6 nanowires/mm²) of small nanowires, which are perpendicular to a silicon substrate and have a length of several tens of micrometers. After the deposition of metal nanoparticles on the top of a silicon wafer, the etch is performed in a solution of HF and an oxidizing agent as H_2O_2 [25–27]. Alternatively, a silicon chip can be etched in a solution of HF and a metal salt, as Silver Nitrate (AgNO_3), which simultaneously acts as oxidizing agent and provides Silver nanoparticles for localized silicon oxidation[27–34]. For the purposes of our work, we have fabricated all the silicon nanowire forests by

means of the latter method, which is simpler because it allows the formation of the structures within a single step. Silicon chips of few centimetres square have been obtained from silicon wafers $\langle 100 \rangle$ oriented, n -doped with a nominal resistivity of 1-10 Ωcm (doping concentration in the range of $5 \times 10^{14} \text{ cm}^{-3}$ and $5 \times 10^{15} \text{ cm}^{-3}$). The nanowire forest fabrication has been performed by soaking the chips in a solution of $\text{HF}:\text{AgNO}_3:\text{H}_2\text{O}$ 16:5:60 in volume[35] (HF 48% in volume, AgNO_3 in solution 0.1 N). This process results in nanowires with a repeatable average diameter of about 90 nm. However, uniformity on large surfaces is an important issue that has to be further investigated in future works. During the etching process for the fabrication of the nanowires, a large amount of Silver nanoparticles are deposited on the sample, as a consequence of the reducing reaction. A complete removal of the Ag nanoparticles has been achieved, after the nanowire fabrication, by soaking the sample in a $\text{HNO}_3:\text{H}_2\text{O}$ solution 1:1 in volume, for 1'. Figure 2 shows SEM images of a typical sample after the etch in $\text{HF}:\text{AgNO}_3:\text{H}_2\text{O}$ 16:5:60 for 120' and the successive removal of Silver nanoparticles by etching in $\text{HNO}_3:\text{H}_2\text{O}$ 1:1 for 1'. The left panel shows the cross-section of the nanowire forest: nanowires with an average diameter of 90 nm are placed perpendicularly to the silicon substrate and have a length of about 20 μm . A planar top view is shown on the right panel. It must be noted that the top ends of the silicon nanowires are bended and tend to group in bundles. However, the bending of the top ends is very small with respect to the total length, so that the nanowires are practically vertical.

We developed a process, based on the electrodeposition of copper, for the fabrication of a common contact at the top of these nanowire forests. At first, a metal seed on top of the nanowires has been provided. The samples have been cleaned in buffered HF (BHF) for 1', in order to remove the thin oxide layer grown during the HNO_3 etch, used for Ag removal. Then, a layer of 15 nm of Cr, which has a good adhesion to the silicon, plus a layer

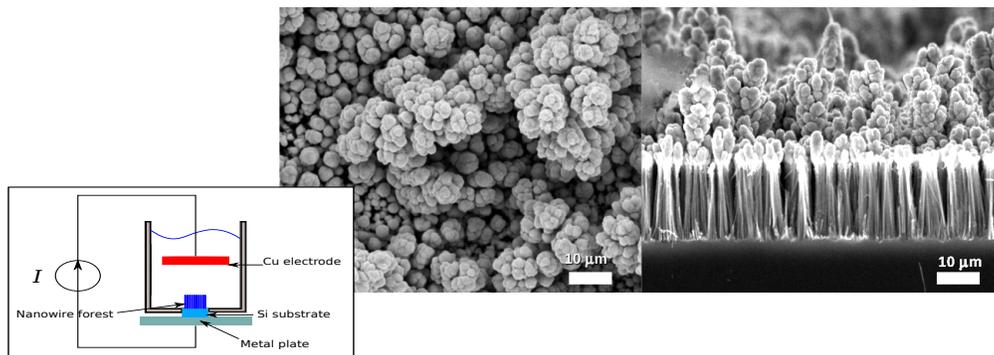


FIG. 3. SEM images of a copper layer grown on the nanowires by electrodeposition in $CuSO_4 : H_2SO_4 : H_2O$ electrolyte, $I=25$ mA, $t=5$ min, planar view on the left panel and cross section on the right. In the inset is shown a sketch of the electrolytic cell with the connection to the current generator.

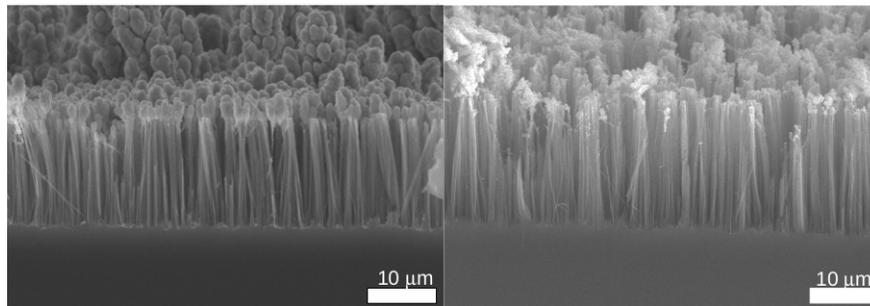


FIG. 4. Comparison between nanowire samples after Cu electrodeposition. Panel left: metal seeds have been deposited by thermal evaporation, before electrodeposition. Panel right: the electrodeposition has been performed with the same solution, current density and time but without pre deposited seeds.

of 20 nm of Cu have been deposited by thermal evaporation. As thermal evaporation is a directional process, the metal is mainly deposited on the top ends of the silicon nanowires. A metal layer has been also provided at the bottom of the sample, on the face opposite to that of the SiNW forest, in order to obtain a good electrical contact of the silicon substrate which is useful for the successive Cu electrodeposition step. A sketch of the electrolytic cell is shown in the inset of the Figure 3: only the nanowire forest is in contact with the electrolytic solution through a hole of 4 mm of diameter. The silicon substrate is connected to the cathode of a current generator, through a metal plate which clamps the sample at the bottom of the cell toward an o-ring seal. The anode of the current generator is connected to a counter-electrode made of a copper plate 1 mm thick. Figure 3 shows SEM images of a typical sample obtained after the growth of Cu by electrodeposition in a solution 0.4 mol/l copper (II) sulfate ($CuSO_4$) and 1 mol/l sulfuric acid (H_2SO_4)[36]. The current was 25 mA (current density of 1989 A/m²) and it has been applied for 5'. From the SEM images is well visible that copper grows only on the top of the silicon nanowires. An accurate investigation through many cross sections made on several samples, prepared in the same conditions, has demonstrated that the selectivity of the growth is very reliable, even if the top ends of the

nanowires are not equally spaced: only very few copper nano particles have been found on the sides near the top of the nanowires.

The main factor which determines the selectivity of the Cu growth is the presence of the metal seed deposited before the electrodeposition process on the top of the nanowires. Figure 4 shows SEM images after copper growth on two similar silicon nanowire forests, one (on the left) with a predeposited seed by means of thermal evaporation and the other (on the right) without the metal seed. The image on the right shows that there is not any copper on the top of the nanowires. On the basis of these experimental results, we think that the selectivity can be ascribed to the localization of the potential drop at the tips of the nanowires, due to their high curvature radius. The metal seed, which is deposited only on the top of the nanowires for the directionality of the thermal evaporation process, enhances this effect and moreover it improves the adhesion, for the presence of the Chromium layer.

II. ROBUSTNESS OF THE PROCESS

The selective growth of copper on the top ends of the silicon nanowires is a very robust and reliable process.

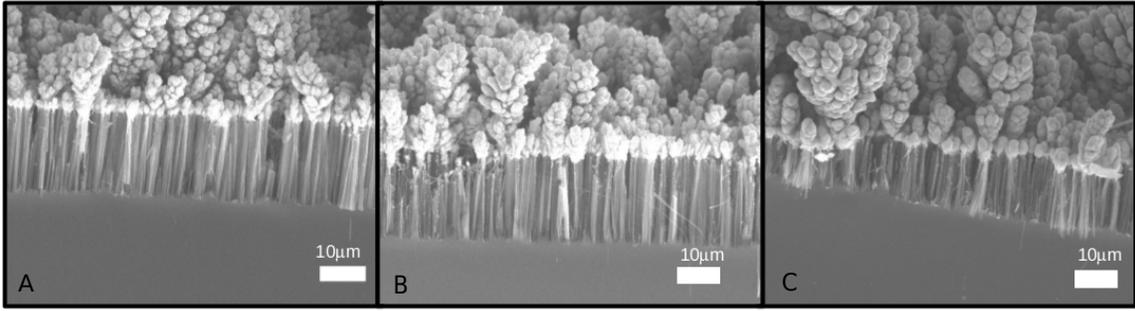


FIG. 5. SEM images of contacted SiNW forests with different Cu growing solution, but with the same current density of 500 A/m^2 , and growth time of 300 sec (total charge of 150 C/m^2). A: CuSO_4 0.4 mol/l and H_2SO_4 1 mol/l, B: CuSO_4 0.2 mol/l and H_2SO_4 1 mol/l, C: CuSO_4 0.8 mol/l and H_2SO_4 1 mol/l.

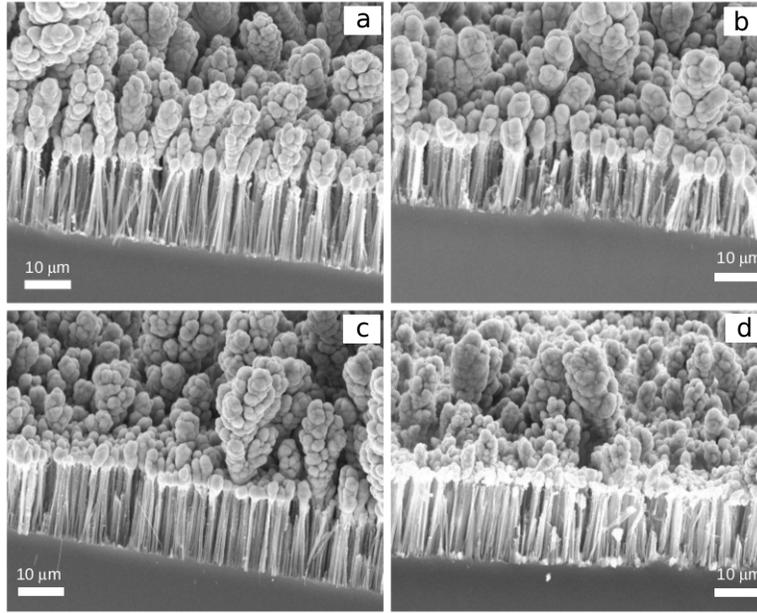


FIG. 6. SEM images of contacted SiNW forests. (a): current density of 398 A/m^2 for 1500 seconds; (b): 637 A/m^2 for 940 seconds; (c): 796 A/m^2 for 750 seconds; (d): 1194 A/m^2 for 500 seconds.

Several experiments have been performed in order to test the effect that the different parameters involved, such as solution concentration, current density and time, have on the electrodeposition process. We group these experiments in three main categories, depending on the process parameter that has been changed: I) different solution concentrations; II) different current densities (with the same charge); III) different deposition times (different charges).

I. At first, the influence of the concentration of CuSO_4 in the electrolyte has been investigated. Solution A, which is made of copper (II) sulfate (CuSO_4) 0.4 mol/l and sulfuric acid (H_2SO_4) 1 mol/l, used for the preparation of the sample in Figure 3, has been chosen as a reference because it has been reported [36] that it generates a copper layer with acceptable resistivity and uniformity. Starting from the solution A, characterized

by a ratio of 0.4 between the concentrations of CuSO_4 and H_2SO_4 , we repeated the process decreasing and increasing the copper concentration, using respectively a solution with $[\text{CuSO}_4]/[\text{H}_2\text{SO}_4]$ ratio 0.2 (solution B) and 0.8 (solution C). Figure 5 shows SEM images of samples prepared with the same current density of 500 A/m^2 and electrodeposition time of 300 s (total charge of 150 C/m^2), but with different electrolytes, corresponding respectively to solution A, B and C. A comparison of these three SEM images shows no significant differences in the copper layer.

II. The effect of current density on the growth of the copper layer has been investigated for currents in the range 160 A/m^2 - 1200 A/m^2 . The total charge has been maintained constant at the value of 7.5 C/m^2 by adjusting the time of the deposition process, so that, accordingly to the Faraday's law, the same quantity of

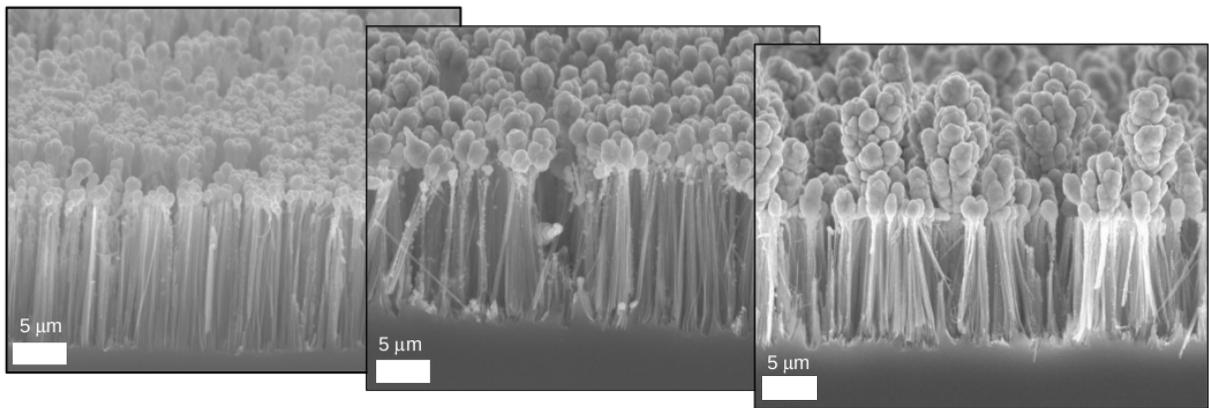


FIG. 7. Contacted SiNW forests with different charge (same current density of 795.77 A/m^2 and increasing time: 15 sec, 60 sec, 600 sec).

copper ($2.47 \cdot 10^{-3} \text{ g/m}^2$) has been grown on the top of the nanowire forests. Figure 6 compares SEM images of cross-sections of four samples, prepared respectively with a current density of 397.9 A/m^2 for 1500 seconds (a), 636.62 A/m^2 for 940 seconds (b), 795.77 A/m^2 for 750 seconds (c), 1193.66 A/m^2 for 500 seconds (d). As well as the experiments with different solutions, we have noticed copper layers comparable to each other.

III. Several samples with different thicknesses of the Cu top layer have been prepared with the same current density, but with different total charge which has been changed by modifying the electrodeposition time. Figure 7 shows cross-sections of SiNW forests with copper grown on the top by applying the same current density of 795.77 A/m^2 for three different times: 15 seconds (left panel), 60 seconds (middle panel), 600 seconds (right panel). As expected, the thickness of the top Cu layer increases with the total charge increasing. These images show clearly that the growth is concentrated on the top ends of the nanowires, starting from “nano-matches” and growing up in the complex configuration shown also in the previous SEM photos.

III. ELECTRICAL CHARACTERIZATION

The Cu grown on the top of a nanowire forest provides a good top contact which is in common with all the nanowires. Four contact measurements of the Cu top layer showed that its conductivity is very high, of the order of $10^6 \Omega^{-1}\text{m}^{-1}$. Therefore, the Cu top layer allows the measurement of the electrical conduction of a large number of parallel nanowires, from the top contact to the silicon substrate at the bottom. It must be noted that there is not any metal connection between the top and the silicon substrate, because copper is grown only on the nanowire vertexes. We measured $I - V$ characteristics of nanowire forests, both low doped and heavily n -doped. Heavily doped nanowires are required for thermoelectric

applications: the optimal doping concentration must be determined on the basis of the nanowire diameter and of the temperature difference[?], but it is always in the range of $10^{18} - 10^{19} \text{ cm}^{-3}$. The fabrication of the nanowire forests, made by means of MaCE, is strongly affected by the doping of the substrate. In particular, we found that MaCE does not give reliable and repeatable results if heavily doped substrates are used as a starting material. Therefore, a good choice is to produce silicon nanowire forests by means of MaCE on low doped substrates, and then the right doping concentration can be successively achieved by means of a suitable doping process. In our case, nanowire forests have been fabricated on silicon substrates with a doping in the range of $5 \times 10^{14} \text{ cm}^{-3}$ and $5 \times 10^{15} \text{ cm}^{-3}$, as reported in Section I, and then they have been doped by means of Phosphorous solid source (ceramic P4700 100 mm X 2 mm, from FILMTRONICS). After MaCE fabrication and Ag nanoparticle removal by HNO_3 etch, samples have been cleaned in buffered HF for removing the thin oxide layer. Samples to be doped have then been placed in a Rapid Thermal Annealer (RTA), with the face containing the nanowires in contact with the solid source, and then they have been heated at $750 \text{ }^\circ\text{C}$ for 5', in N_2 atmosphere. After the doping process, the Cu growth has been performed following the procedure illustrated in section II (deposition of the metal seed by thermal evaporation followed by Cu electrodeposition). By SEM inspection, we cannot appreciate any significant difference between the Cu layers grown with the same electrodeposition parameters on doped or on undoped samples. This implies that the electrodeposition process does not depend on the electrical conductivity of the silicon nanowires.

Figure 8 shows, on the left panel, typical $I - V$ characteristics of doped and undoped nanowire forests, measured between the top Cu layer and the bottom silicon substrate. In the inset on the right panel a sketch of the measurement set-up is shown: the substrate is contacted through the metal layer already used for the electrodeposition process (see the sketch in Fig. 3). Silver colloidal

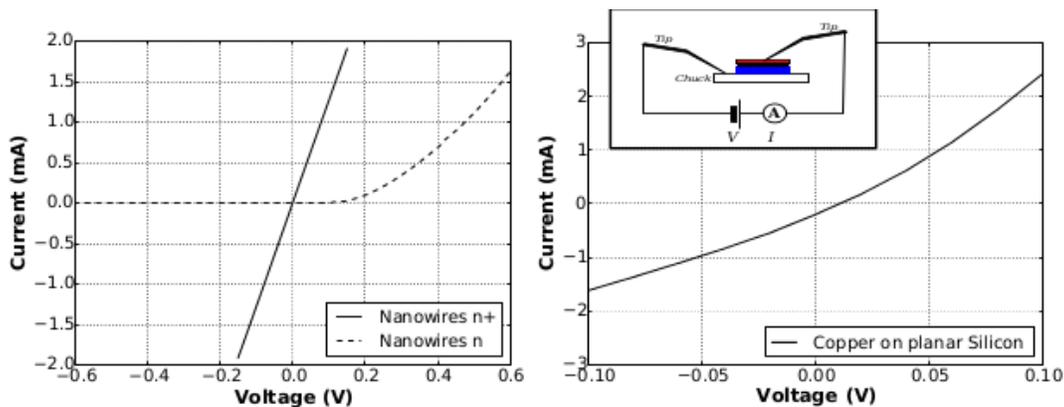


FIG. 8. Panel left: $I - V$ characteristic on a sample of nanowires n -doped and nanowires $n+$ -doped. Panel right: $I - V$ characteristic of copper on planar Silicon. On the inset: the measurement apparatus.

paste has been deposited on the Cu layer at the top of the sample, in order to achieve a planar surface and a more uniform electrical contact with a micromanipulated tip. It is evident, from Fig. 8, that the undoped nanowire forest shows a rectifying behaviour: it behaves like a Schottky diode, typical of a metal contact deposited on a moderately n -doped silicon substrate. The behaviour of the doped silicon nanowire forest is instead linear (resistive): not any barrier effect is observed, as typical for a metal contact on a heavily doped silicon. On the right panel of Fig 8, the characteristic of a silicon sample with a Cu layer grown on top, but without nanowire forest, is reported for comparison: an almost symmetric behaviour is shown. From this last measurement, knowing the geometrical dimensions of the sample (the surface is about a centimetre square, the thickness is 0.5 mm), it is possible to estimate the resistivity of the substrate which is of 4 Ω cm. This value is compatible with the nominal wafer resistivity of 1-10 Ω cm.

IV. CONCLUSIONS

A large number of vertical silicon nanowires can be achieved both by epitaxial growth and by selective vertical etching. An important issue for the production of any kind of device, based on these silicon nanowire forests, is the fabrication of reliable electrical (and thermal) contacts. One end of the silicon nanowires is anchored to the silicon substrate, which is a good electrical and thermal conductor. The difficult issue is to fabricate a contact to the other end, at the top of the silicon nanowires. We have presented a cheap and reliable process for the deposition of a Cu layer to the top end of a silicon nanowire forest. The process has been developed on silicon nanowire forests achieved by Metal-assisted Chemical Etching, and it is based on copper electrodepo-

sition. The stability and repeatability of the Cu growth, which is selective onto the top ends of the nanowires, have been tested for a large range of the parameters involved in the process (solution concentration, current density, and total deposited charge). A key point for the selective Cu growth is a starting Cr/Cu layer deposited on top of the silicon nanowires by means of a directional thermal evaporation. $I - V$ characteristics of a large number of parallel nanowires have been measured both on n -doped and on heavily doped forests, contacted by means of the presented technique.

The process improved in our work is an important and essential step for several applications, such as thermoelectric generation which could exploit the low thermal conductivity of silicon nanowires to achieve high conversion efficiencies. Several experimental works have been devoted in the past to the measurement of the SiNW thermal conductivity. These works have clearly demonstrated the potentialities of nanostructured materials for energy harvesting applications. However, the devices that have been used for these measurements were based on a single (or very few) silicon nanowire, and for this reason these devices are not suitable for practical applications. The fabrication of a contact on a huge number of nanowires, produced by a simple and cheap technique, offers the opportunity for the production of devices capable of handling and delivering a considerable amount of power, therefore these devices could be employed in many practical applications.

Future work is needed, at first, for the fabrication of uniform silicon nanowire forests on surfaces as large as possible. Moreover, even if we demonstrated that it is possible to tailor the doping of silicon nanowires after their fabrication, several experimental works are needed for solving problems related with the mechanical, thermal and electrical assembly of n -doped and p -doped silicon nanowire forests.

-
- [1] L. Wei, P. Xie, and C. Lieber, *IEEE trans. electron. dev.* **55**, 2859 (2008).
- [2] J. Fu, N. Sing, K. Buddharaju, H. Teo, S. C. Y. Jiang, C. Zhu, M. Yu, G. Lo, N. Balasubramanian, D. Kwong, E. Gnani, and G. Baccarani, *IEEE electron. dev. Lett.* **29**, 518 (2008).
- [3] Y. Cui, Q. Wei, H. Park, and C. Lieber, *Science* **293**, 1289 (2001).
- [4] A. Talin, L. Hunter, F. Leonard, and B. Rokad, *Appl. Phys. Lett.* **89**, 153102 (2006).
- [5] B. Tian, X. Zheng, T. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, and C. Lieber, *Nature Letters* **449**, 885 (2007).
- [6] P. Hiralal, H. E. Unalan, and G. Amaratunga, *Nanotechnology* **23**, 194002 (2012).
- [7] V. Sivakov, G. Andra, A. Gawlik, A. Berger, J. Plentz, F. Falk, and S. Christiansen, *Nano Letters* **9**, 1549 (2010).
- [8] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, and A. Majumdar, *Appl. Phys. Lett.* **83**, 2934 (2003).
- [9] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, C. E. Garnett, M. Najarian, A. Majumdar, and P. Yang, *Nature Letters* **451**, 163 (2008).
- [10] Y.-H. Park, J. Kim, H. Kim, I. Kim, K. Y. Lee, D. Seo, H. J. Choi, and W. Kim, *Applied Physics A* **104**, 7 (2011).
- [11] J. Lim, K. Hippalgaonkar, S. Andrews, C., A. Majumdar, and P. Yang, *Nano Letters* **12**, 2475 (2012).
- [12] P. Martin, Z. Aksamija, E. Pop, and U. Ravaioli, *Phys. Rev. Lett.* **102**, 125503 (2009).
- [13] J. Carrete, L. Gallego, and L. Varela, *Phys. Rev. B* **84**, 075403 (2011).
- [14] G. Pennelli and B. Pellegrini, *J. Appl. Phys.* **101**, 104502 (2007).
- [15] K. Moselund, D. Bouvet, M. Jamma, D. Atienza, G. Leblebici, G. DeMicheli, and A. Ionescu, *Microelectron. Eng.* **85**, 1406 (2008).
- [16] G. Pennelli, *Microelectronic Engineering* **86**, 2139 (2009).
- [17] Y. Cui, L. Lauhon, M. Gudiksen, J. Wang, and C. Lieber, *Appl. Phys. Lett.* **78**, 2214 (2001).
- [18] V. Schmidt, S. Senz, and U. Gosele, *Nano Letters* **5**, 931 (2005).
- [19] G. Pennelli, M. Totaro, M. Piotto, and P. Bruschi, *Nano Lett.* **13**, 2592 (2013).
- [20] M. Totaro, P. Bruschi, and G. Pennelli, *Microelectron. Eng.* **97**, 157 (2012).
- [21] Z. Huang, N. Geyer, P. Werner, J. de Boor, and U. Gosele, *Advanced Materials* **23**, 285 (2011).
- [22] J. Kim, H. Han, Y. Kim, S.-H. Choi, J.-C. Kim, and W. Lee, *ACS nano* **5**, 3222 (2011).
- [23] T. Zhang, S. Wu, R. Zheng, and G. Cheng, *Nanotechnology* **24**, 505718 (2013).
- [24] J. Weisse, A. Marconnet, D. Kim, P. Rao, M. Panzer, K. Goodson, and X. Zheng, *Nanoscale Research Letters* **7**, 554 (2012).
- [25] X. Li and P. Bohn, *Applied Physics Letters* **77**, 2572 (2000).
- [26] . Ming-Liang Zhang, . Kui-Qing Peng, . Xia Fan, . Jian-Sheng Jie, . Rui-Qin Zhang, . Shuit-Tong Lee, , and . Ning-Bew Wong*, *The Journal of Physical Chemistry C* **112**, 4444 (2008).
- [27] Z. Huang, N. Geyer, P. Werner, J. De Boor, and U. Gösele, *Advanced materials* **23**, 285 (2011).
- [28] C.-Y. Chen, C.-S. Wu, C.-J. Chou, and T.-J. Yen, *Advanced Materials* **20**, 3811 (2008).
- [29] A. G. Nassiopoulou, V. Gianneta, and C. Katsogridakis, *Nanoscale research letters* **6**, 1 (2011).
- [30] K. Peng, H. Fang, J. Hu, Y. Wu, J. Zhu, Y. Yan, and S. Lee, *Chemistry—A European Journal* **12**, 7942 (2006).
- [31] K. Peng, Y. Yan, S. Gao, and J. Zhu, *Advanced Functional Materials* **13**, 127 (2003).
- [32] K.-Q. Peng, Y.-J. Yan, S.-P. Gao, J. Zhu, *et al.*, *Advanced Materials* **14**, 1164 (2002).
- [33] K. Peng, J. Hu, Y. Yan, Y. Wu, H. Fang, Y. Xu, S. Lee, and J. Zhu, *Advanced Functional Materials* **16**, 387 (2006).
- [34] K. Peng, Y. Xu, Y. Wu, Y. Yan, S.-T. Lee, and J. Zhu, *small* **1**, 1062 (2005).
- [35] C.-Y. Chen, C.-S. Wu, C.-J. Chou, and T.-J. Yen, *Advanced MAterials* **20**, 3811 (2008).
- [36] N. N. Le, T. C. H. Phan, A. D. Le, T. M. D. Dang, and M. C. Dang, *Advances in Natural Sciences: Nanoscience and Nanotechnology* **6**, 035007 (2015).