Potentialities of silicon nanowire forests for thermoelectric generation

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Abstract

Silicon is a material with very good thermoelectric properties, with regard to Seebeck coefficient and electrical conductivity. Low thermal conductivities, and hence high thermal to electrical conversion efficiencies, can be achieved in nanostructures which are smaller than the phonon mean free path but large enough to preserve the electrical conductivity. We demonstrate that it is possible to fabricate a leg of a thermoelectric generator based on large collections of long nanowires, placed perpendicularly to the two faces of a silicon wafer. The process exploits the metal assisted etching technique which is simple, low cost, and can be easily applied to large surfaces. Copper can be deposited by electrodeposition on both faces, so that contacts can be provided. Thermal conductivity of silicon nanowire forests with more than 10^7 nanowires/mm^2 has been measured; the result is comparable with that achieved by several groups on devices based on few nanowires. On the basis of the measured parameters, numerical calculations of the efficiency of silicon-based thermoelectric generators are reported, and the potentialities of these devices for thermal to electrical energy conversion are shown. Criteria to improve the conversion efficiency are suggested and described.

Keywords: nanowires, thermoelectricity, metal assisted chemical etching, electrodeposition

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The direct conversion of heat into electrical power, through thermoelectric generation, is very attractive for the recovery of waste heat and hence for green energy harvesting and for energy scavenging. However, at the present state of the art, the applications of thermoelectric conversion are still very limited because conventional thermoelectric materials are based on tellurium which is a rare and poisoning element. Materials with good thermoelectric properties but also which are biocompatible, affordable, technologically feasible, need to be developed for an extensive application of thermoelectric devices. A possible break-through would be established if silicon, which is abundant on the Earth's crust and biocompatible, could be used. Moreover, silicon is very well known from the technological point of view, and techniques for doping it and for the fabrication of contacts are largely assessed. Furthermore, silicon is very stable on a large range of temperatures. Therefore, it could be suitable for applications which exploit small temperature differences, as energy scavenging, and from applications of energy recovery from high temperatures heat sources.

In section I we review the main works on the measurement of the silicon Seebeck coefficient, and we discuss the potentialities of silicon as thermoelectric material, underlining that the main limitation is its high thermal conductivity. The aim is to demonstrate the importance of the development of nanostructured silicon devices for high efficient thermal to electrical energy conversion. As demonstrated by several experimental works[1, 2, 3], thermal conductivity is strongly reduced in nanostructured silicon. A clear relationship between the roughness of the surfaces of silicon nanowires and the reduction of phonon conduction due to the surface scattering has been established[4, 5]. All these works are of paramount importance because demonstrate that materials, such as silicon, with high thermal conductivity in their bulk status can be used for thermoelectric applications when nanostructured. However, all these works are based on devices made of one, or very few, nanowires; hence, the total current that these devices can deliver is very small. A thermoelectric generator useful for practical

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applications must handle a considerable amount of current, therefore it must consists on a large number of interconnected nanostructures. The main point that we address in section II is the development of techniques for the fabrication of huge collections of interconnected silicon nanowires. In particular, we describe the fabrication process for one leg of a thermoelectric generator based on silicon nanowire forests, and we report data on the thermal conductivity of a large number of parallel nanowires. Our top-down process is based on Metal Assisted Chemical etching, which is a cheap and simple technique for the fabrication of vertical nanowires on large silicon areas. We show that the series parasitic electrical resistance, introduced by the substrate, can be reduced by using a double face silicon etching. In section III we report the results of finite-element modeling of the maximum efficiency of thermoelectric generators based on nanowire forests. Strategies for reducing the effect of the parasitic electrical resistance introduced by the substrate are illustrated and discussed.

1. Properties of silicon as thermoelectric material

The potentialities of a thermoelectric material are in general expressed by the parameter $Z = S^2\sigma/k_t$, or by the non-dimentional figure of merit ZT, where S is the coefficient of Seebeck, σ is the electrical conductivity and k_t is the thermal conductivity. A good thermoelectric material should have Z as high as possible, which means high values of S and σ, and low values of the thermal conductivity k_t. Silicon exhibits interesting values of the Seebeck coefficient S and of the electrical conductivity σ. The main limitation of silicon for thermoelectric applications is its high k_t, which is 148 W/(m K). Both S and σ depend on the doping type (n or p) and concentration, and on temperature. The electrical conductivity σ has been extensively investigated in the past years for the large used of silicon in the fabrication of integrated circuits. On the basis of all these studies, semi-empirical formulas, as the one derived by Arora[6], have been developed for the evaluation of σ. These formulas are largely used for the numerical simulations of electron devices; in particular, we used the Arora's formula for our estimations of the potentialities of TEGs based on silicon of

Sec. IV. On the other hand, very few experimental measurements are available for the Seebeck coefficient of silicon. We based our estimations of S on the works of Geballe and co-workers[7], Brinson and Dunstant[8], and on the more recent works of Stranz and co-workers[9] and Bennett[10]. We reported these experimental measurements (extracted by the graphs shown in the cited papers) in the left panel of Figure 1. The formula of Stratton (for n doping):

$$S = -\frac{k}{q}\left(\frac{5}{2} - ln\frac{n}{N_C}\right)$$

where k is the Boltzmann's constant, q is the elementary charge, n is the electron concentration and N_C is the equivalent density of states, assumes a logarithmic dependency of S from the doping concentration, but gives values which are underestimated for high doping concentrations where the approximations needed for the correct application of N_C are not valid anymore[3]. However, it must be noted that the power factor $S^2\sigma$ has a maximum for high doping concentrations, hence the Stratton's formula is not suitable for the evaluation of thermoelectric performances. Therefore, we assumed a logarithmic dependency of S from the doping but we used a fit of the available experimental data: the logarithmic fit is shown together with the data in the left panel of Fig. 1. In the right panel of Fig. 1 we report the power factor $S^2\sigma$ as a function of the n doping concentration, at room temperature, evaluated with the Arora's formula (for the electrical conductivity) and using the logarithmic fit of the left panel for the S values. The power factor depends on doping and it is maximum for a n doped concentration of about 5×10^{19} cm^{-3}[10].

Figure 2 shows the product $S^2\sigma T$ as a function of temperature for two different values of n doping concentration. This coincides with the figure of merit if an ideal value of $k_t = 1$ W/(m K) is assumed ($ZT = S^2\sigma T\frac{1}{k_t}$). The values for $\sigma(n, T)$ have been obtained again with the Arora's formula[6]. For the doping concentration $n = 1.4 \times 10^{19}$ cm^{-3}, $S(T)$ has been determined with a polynomial fit of the data extracted from the work of Stranz and co-workers[9]. The other doping concentration $n = 5 \times 10^{19}$ cm^{-3} has been chosen because, as it can be seen from Fig. 1, the maximum of the power factor, at room temperature,

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is obtained for n very close to this value. In this case, the behavior of S as a function of temperature has been extrapolated by the experimental results available for $n = 1.4 \times 10^{19}$. The graphs of Fig. 1 and of Fig. 2 demonstrate the great thermoelectric potentialities of silicon if a strong reduction of the thermal conductivity is achieved. The electron transport is practically unaffected by the surface scattering in heavily doped nanowires with a diameter D wider than 50 nm[3, 11]. This is because the electron mean free path in heavily doped silicon is very small, of the order of few nanometers, as the scattering of electrons is principally due to the doping impurities. Therefore, the electrical resistance and the Seebeck coefficient of nanowires with $D > 50$ nm are the same as that of bulk silicon. Conversely, a thermal conductivity of few W/(m K) has been measured[12, 4] for silicon nanowires with diameters between 50 nm and 100 nm. This is because the phonon mean free path is of the order of several tens of nanometers, hence it is larger than that of the electrons. Therefore, the diameter range 50 nm $< D < 100$ nm is suitable for nanowires with the same electrical characteristics, and in particular with the same power factor than that of bulk silicon, but with a reduced thermal conductivity. For these reasons, such silicon nanowires are very promising for the fabrication of high efficient thermoelectric generators.

2. Thermoelectric generators based on silicon nanowire forests

As pointed out in the previous section, several research groups have demonstrated the reduction of the thermal conductivity in devices based on few nanostructures. However, the exploitation of the enhanced thermoelectric potentialities at the nanoscale requires the development of techniques for the reliable fabrication of a huge number of interconnected nanostructures. Thermoelectric generators, based on these collections of nanostructures, could deliver the high currents and powers required by practical applications.
A possible strategy consists in the use of advanced optical (or e-beam) lithography, combined with standard silicon processing techniques, for the fabrication of large arrays of nanowires in the top layer of a Silicon On Insulator wafer[13, 11].

This horizontal (planar) strategy has at least two important drawbacks. At first, complex techniques for the suspension of networks of nanostructures need to be developed[14], in order to avoid the parasitic thermal conduction of the substrate. Moreover, it relies on high resolution lithography, and for this reason techniques based on this planar strategy are very expensive.

Another possible strategy is to exploit highly selective silicon etching for the fabrication of nanowires which are perpendicular to a silicon wafer. Highly selective plasma etching can be used to this end. However, the length of the nanowires relies on the selectivity of the etch: the aspect ratio of the most selective deep reactive ion etching technique is not greater than 100:1[15], which means a nanowire length of 10 μm for a diameter of 100 nm. Vertical nanowires can be fabricated also by bottom-up approaches, as for example Vapor Liquid Solid (VLS) epitaxy [16, 17] We developed a process based on a very promising technique, which is the metal-assisted chemical etching[18, 19, 20, 21] (MACE). This technique is simple and low-cost because it can be performed without expensive lithography and complex growth machines, giving nanowire forest on large area samples. The MACE is highly selective allowing the fabrication of silicon structures, perpendicular to a standard silicon wafer with a very high aspect ratio. We use a one step technique that consists in soaking a (100) oriented silicon wafer in a solution with hydrofluoric acid (HF) and silver nitrate ($AgNO_3$). In the same step, silver nanoparticles are deposited on the wafer surface for the reduction of the salt, and then these nanoparticles act as localized catalytic centers for silicon etching. With this MACE technique, more than 10^7 nanowires/mm^2, with a random diameter in the range 60 nm $< D <$ 90 nm (see the left panel of Fig. 3) can be easily fabricated on surfaces of several cm^2 . Even if the nanowire diameter is not constant, its dispersion is in the interesting range for the exploitation of the thermal conductivity reduction. Therefore, nanowire forests obtained by MACE are very promising for the fabrication of thermoelectric generators with high conversion efficiencies. In a previous work[22], we faced the key point of the fabrication of a contact on the top of a nanowire forest. We demonstrated that copper can be selectively grown on the apexes of the

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nanowires by electrodeposition, once provided a seed by thermal evaporation (see the right panel of Fig. 3). The bottom contact is provided by the silicon substrate.

Several nanowire forests have been grown with different nanowire lengths, which depends on the process parameters and in particular on the etch time. We easily reached nanowire lengths of more than 70 μm using suitable concentrations, etching times and solution volumes. The latter parameter is important because Ag is reduced and deposited on the surface during the etch, therefore the Ag concentration in the solution decreases with time. As for example, the nanowire forests shown in the SEM images of Figure 3 have been fabricated by etching a (100) Si n-doped wafer (ρ $1 - 5$ Ω cm), in a solution 2:16:60 AgNO$_3$:HF:H$_2$O for four hours. After the MACE, silver has been removed by an etch in a 1:1 HNO$_3$:H$_2$O solution for 2 minutes. Then, a copper layer has been grown in 0.4 mol/L CuSO$_4$ and 1 mol/L H$_2$SO$_4$ electrolytic solution, applying a current density of 2000 A/m^2 for 5 minutes: the final result is shown in the right panel of Fig. 3. Finally, the copper surface has been polished and planarized by silver paste, in order to increase the thermal conductivity of the contact.

Thermal conductance measurements have then been performed by the guarded hot plate technique, on samples of about 2×2 mm^2 of surface. Samples with nanowire forests of different lengths, between 7 and 50 μm, have been fabricated on Si substrates 500 μm thick. Lengths have been accurately measured by SEM images. The real cross-section area of the nanowire forests, which is smaller than the total area of the sample, has been estimated by several SEM images taken in different areas on the same sample. In this way, the ratio ν between the nanowire forest cross-section area and the total area of the sample has been estimated, and it resulted of about 0.3 for all the fabricated samples. We called the parameter ν the coverage ratio of the silicon nanowire forest. The thermal resistance, which is the ratio between the temperature drop and the thermal power flux, has been measured heating the guarded hot plate on top of the sample to a temperature of 45 ^{o}C, and maintaining the bottom temperature at 30 ^{o}C. Temperatures have been measured by means of Pt100 sensors, and the ap-

plied power flux was 1.5 W. The measured thermal resistance is due to the series of the nanowire forest, of the substrate and of the contact resistance. The latter has been assumed the same for all the measured sample. For the substrate, the thermal conductivity of bulk silicon (148 W/m K) has been assumed. The total thermal resistance increases with the increasing of the nanowire length. Therefore, the difference of the thermal resistance between samples has been ascribed to the different length of the nanowires. Comparing the the thermal resistance of different samples, knowing the geometrical factors (length and cross-section area), a thermal conductivity of about 3 W/(m K) has been derived. This value, which we measured on large area nanowire forests, is in agreement with that measured by several groups on single silicon nanowires[2, 4].

This data is very promising for thermoelectric applications. The nanowire forests can be doped after their fabrication by standard doping diffusion, and high doping concentrations, either p^+ or n^+, can be achieved. Therefore, both n^+ and p^+ legs of a thermoelectric generator, based on silicon nanowire forests, can be fabricated and interconnected through the top copper layer and the bottom substrate. The main drawback of the vertical strategy is the substrate itself which introduces an electrical resistance in series to that of the nanowires. This parasitic electrical resistance decreases the efficiency of the thermoelectric generator (see the next section). Unfortunately, the MACE process does not give satisfying results on heavily doped (n^+ and p^+) substrates. MACE gives good monocrystalline silicon nanowires for substrates with $n < 10^{17}$ cm^{-3} [23, 24]. In our experiences, we have not found any suitable [HF]/[AgNO$_3$] concentration ratio for achieving good nanowire forests on heavily doped substrate: we found either that the etch proceeds in all directions (not only vertically), or that the nanowires are very porous. This confirms the results obtained by Schmid and co.workers[23] with a two-step MACE. From these studies, it seems that the only possible path to obtain highly doped silicon nanowire forests is to dope them by thermal diffusion after the etching. Therefore, we have to face the problem of the substrate that remains moderately doped and introduces an electrical resistance in series with the nanowires.

This parasitic resistance deteriorates the thermal to electrical conversion efficiency of the system.

A possible way to reduce the effect of the electrical resistance of the substrate is to exploit the MACE for etching silicon nanowire forests on both faces of a double polished wafer. The total length of the nanowires doubles and simultaneously the thickness of the substrate is reduced. The SEM image of Figure 4 shows silicon nanowire forests achieved by MACE etching of a double polished wafer 500 μm thick. A silicon chip with a surface of roughly 1×1 cm^2 has been soaked in a solution 5:16:60 AgNO$_3$:HF:H$_2$O for 2 h. The chip was hold by a plastic clamp applied to one edge, and it was randomly moved by an automatic handler to provide a stirring of the solution and a better uniformity of the etch on both surfaces. As expected, the MACE proceeds simultaneously on both faces of the sample, giving as a result nanowire forests on each surface. If the maximum reachable nanowire length is indicated by L_{max} (as for example 70-80 μm), this technique yields samples with nanowire forests which are in series, and therefore which have a total equivalent length of $2L_{max}$ (more than 150 μm). Figure 5 shows two SEM images of nanowire forests achieved on both sides of a silicon wafer 200 μm thick. The wafer has a resistivity of 10 Ωcm, and it has been etched for 4 h in a solution of 4:32:120 AgNO$_3$:HF:H$_2$O, (photo on the left panel) and in a solution 8:64:240 AgNO$_3$:HF:H$_2$O (photo on the right panel): only few tens of micrometers of low doped substrate remained. A copper layer can be grown on both faces, repeating for two times the electrodeposition process illustrated above[22]. Figure 6 shows the nanowire forests on both faces with the two copper layers grown on the nanowire apexes. After the MACE etching process, and before the Cu growth, both forests have been heavily n doped with phosphorous by thermal diffusion. Figure 7 shows an $I - V$ characteristic measured between the top and the bottom Cu contacts of the double side nanowire forests, shown in Fig .6. Both faces have been planarized with silver paste before the measurement. A linear fit of the $I - V$ characteristic of Fig. 7 gives a resistance of 22 Ω, which is essentially the resistance of the remaining substrate 30 μm thick.

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3. Expected thermoelectric performances of silicon nanowire forests

In order to give an estimation of the potentialities of silicon nanowire forests, we performed some finite-element calculations on the basis of the measured values of the Seebeck coefficient, reported by the literature (see Sec. II), and of the thermal conductivity of nanowires. At first, we determined the thermal to electrical conversion efficiency of silicon nanowires in the ideal case of absence of substrate. We considered a temperature difference $T_{Hot} - T_{Cold}$ ($T_H - T_C$) directly applied between the ends of the nanowires. Figure 8 shows the maximum thermal to electrical conversion efficiency (calculated by Finite-Element) of the hot side temperature T_H, for a cold side temperature $T_C = 300$ K. We considered nanowires n-doped 5×10^{19} cm^{-3} because, as shown in Section II, the silicon power factor is maximum for a doping concentration close to this value. The dependency on temperature of the thermoelectric parameters ($S(T)$, $\sigma(T)$ and $k_t(T)$) has been taken into account as described in Sec. II. The efficiency is a function of the current density which flows in the nanowires, so the current which gives the maximum efficiency has been determined for each value of the high temperature T_H ($T_C = 300$ K). At first, we developed a Python function which evaluates the efficiency by solving the non linear thermoelectric equations for a given current density. To this end, we used the FENICS[25, 26, 27] Finite-Element package to solve the 1D thermoelectric equations[28, 14]:

$$
\begin{aligned}
J &= \sigma \mathcal{E} - S\sigma \frac{dT}{dx} \\
\phi &= STJ - k_t \frac{dT}{dx}
\end{aligned}
$$

where J is the current density, $\mathcal{E}$ is the electric field and ϕ is the heat flux. These equations have been solved simultaneously with the continuity equation for the electrical current and the heat equation (V is the electrical potential):

$$
\begin{aligned}
\frac{dJ}{dx}(V,T) &= 0 \\
\frac{d\phi}{dx}(V,T) &= -\frac{dV}{dx}J(V,T)
\end{aligned}
$$

Then, we implemented a golden section search algorithm[29] which uses this function to find the current density for the maximum efficiency. The two curves of Fig. 8 shows the maximum efficiency as a function of T_H for two values of the thermal conductivity k_t. The value of $k_t = 3$ W/(m K) has been measured on our nanowire forests, meanwhile $k_t = 1$ W/(m K) is an optimistic value which could be eventually obtained with processes for the increasing of the nanowire roughness. The Carnot efficiency for the given temperature difference $T_H - T_C$ is also reported for a comparison. As expected, the efficiency increases with the decreasing of the thermal conductivity, and values in excess of 30 % can be obtained for $T_H = 800$ K. However, interesting efficiency values (about 23 % for $T_H = 800$ K) can be reached also with the measured k_t value of 3 W/(m K).

In Figure 9 we show a comparison between the maximum efficiency achievable with nanowire forests built on a single-face polished wafer (left panel) and nanowire forests built on double-face polished wafer (right panel), as a function of the doping of the substrate. In both graphs, for the nanowires it has been considered: a doping concentration $n = 5 \times 10^{19}$ cm^{-3}; the experimental value of 3 W/(m K) for k_t. For the substrate, the thermal conductivity of bulk silicon $k_t = 148$ W/(m K) has been taken into account. A 1D FEM calculation has been performed. The different cross section area between the substrate and the nanowire forest has been taken into account scaling the current density J and the heat flux ϕ with the coverage ratio ν. The experimental value of $\nu = 0.3$ has been used for the results shown in Fig. 9. The top and the bottom temperatures have been fixed at $T_H = 800$ K and $T_C = 300$ K (see the insets). Several curves have been calculated for different nanowire lengths. The sum of the nanowire length and the thickness of the substrate is fixed at 200 μm, therefore the structures are similar to those achievable by etching for different times a silicon wafer 200 μm thick. In both graphs, the ideal efficiency achievable with substrate-free nanowires forests, which is 23 % for the temperature difference $T_H - T_C = 800 - 300$ K, is reported for comparison. As expected, the efficiency increases with the increasing of the doping concentration of the substrate and with the decreasing of the substrate thickness. However, in the case of the

single face structures the efficiency is very low with respect to the ideal one, even for highly doped substrates. Instead, reasonably high efficiencies can be achieved with the double face nanowire forests. Moreover, in the case of single face nanowire forests the efficiency has a strong increase in all the doping range. On the contrary, for double face nanowire forests, in particular for $L_{nw} = 90$ μm and $t_{sub} = 20$ μm, the efficiency strongly increases for doping concentration up to about 10^{18} cm^{-3}, then the curve tends to saturate. Therefore, a great enhance of the efficiency can be achieved just making possible the fabrication of nanowire forests on substrates with doping concentrations up to that value. The fabrication of nanowire forests on substrates with higher doping values are advantageous but the efficiency shows only a limited increase.

A possible parameter for the optimization of the efficiency is the coverage ratio ν. With the MACE parameters used in our processing, we measured $\nu = 0.3$ after the etch of the forest. This value can eventually be decreased after the fabrication of the nanowire forests by a masked etching, to be performed with further processing to be developed. Figure 10 shows the efficiency for a double nanowire forest with $L_{nw} = 90$ μm and $t_{sub} = 20$ μm, as a function of the doping of the substrate. Different curves are related to different values of ν. As expected, the efficiency increases with the decreasing of the coverage ratio. This is because the resistance of the nanowire forests increases for the same resistance of the substrate, therefore the effect of the substrate resistance is smaller. However, this via to increase the efficiency has an important drawback: the effective area of the nanowires decreases with ν, with respect to the cross section area of the device which is that of the substrate. Therefore, larger devices must be used to deliver the same total current.

4. Conclusions

We demonstrated that it is possible to fabricate legs for thermoelectric generators based on large collections of silicon nanowires, placed perpendicularly to a silicon substrate (silicon nanowire forests. A cheap and simple selective MACE vertical etching can be used for the fabrication of nanowire forests on

both faces of a silicon wafer, achieving a total nanowire length of more than 150 μm. A copper layer can be grown on the top of both forests to provide the thermal and electrical contact. The measured thermal conductivity, measured on the overall nanowire forests, is comparable to that reported by several groups on single nanowires. FEM simulations demonstrated the high conversion efficiencies which can be achieved with these devices. Hence, thermoelectric generators based on nanowire forests are very promising for direct thermal to electrical conversion applications.

Further experimental work is necessary for the fabrication of a complete thermoelectric generator made of several modules both n and p doped. In particular, even if contacts are provided by the copper layer, strategies for the reduction of the thermal contact resistance and for the interconnection and the assembly of different modules need to be developed. After that, a full characterization of the thermoelectric generator could give a confirmation of the predicted efficiencies.

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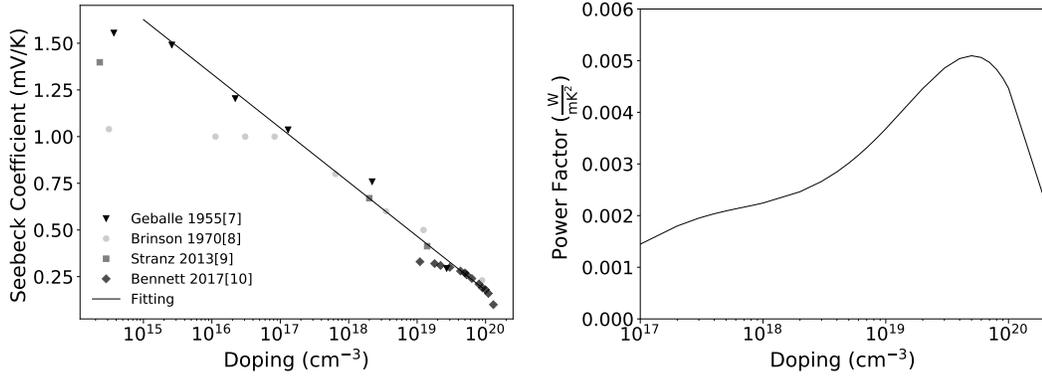
Figure 1: Left panel: experimental data, together with a logarithmic fit, of the Seebeck coefficient of silicon, at room temperature, extracted by the papers reported in the legend. Right panel: power factor $S^2\sigma$ of silicon as a function of doping, at room temperature, evaluated with the Arora's formula (for the electrical conductivity) and using the logarithmic fit of the left panel for the S values.
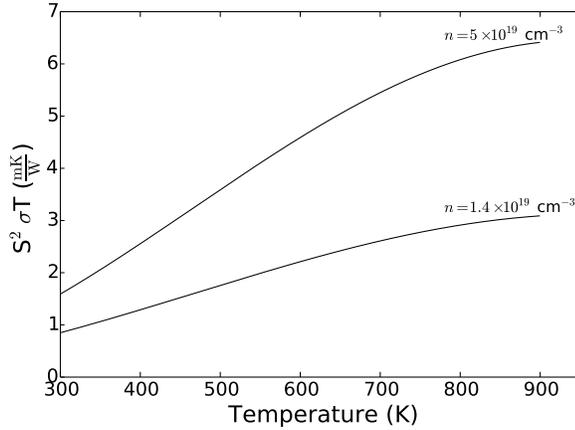

Figure 2: The figure of merit ZT of silicon, multiplied by the thermal conductivity k_t, is shown as a function of temperature.
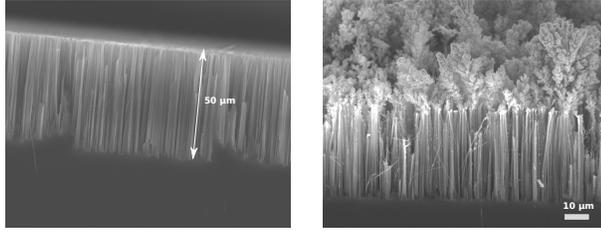
Figure 3: Left panel: SEM photo of nanowires perpendicular to a silicon substrate, achieved by MACE. Right panel: SEM photo showing the copper grown by electrodeposition on the top of the silicon nanowire forest.
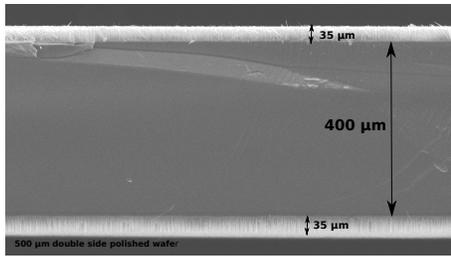
Figure 4: Silicon nanowire forest on both sides of a double polished wafer(n type, thickness 500 μm, 2 hours etch).
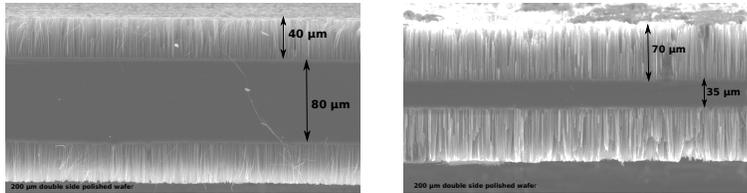
Figure 5: Silicon nanowire forests obtained by etching a double polished wafer (p type, thickness 200 μm, 4 hours etch). A solution 4:32:120 AgNO$_3$:HF:H$_2$O and 8:64:260 AgNO$_3$:HF:H$_2$O has been used, respectively, for the left and right sample.
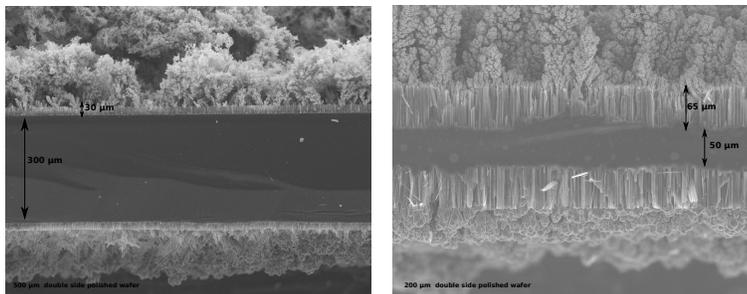
Figure 6: The two SEM images show the copper layers grown on the apexes of the nanowire forests on both faces of the wafer.

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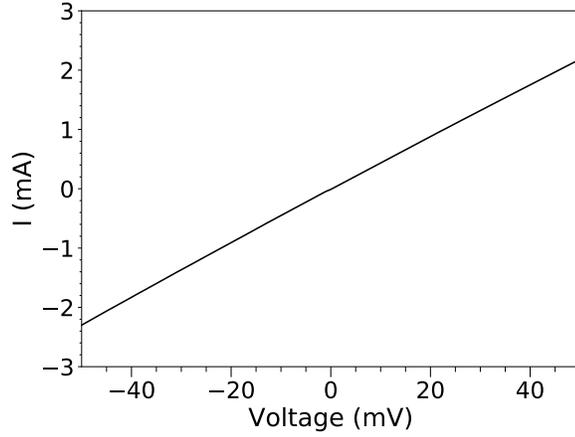
Figure 7: $I - V$ characteristic of a double silicon nanowire forest. The two nanowire forests have a length of about 70 μm, the remaining substrate is about 30 μm thick and it has a resistivity of 10 Ωcm. Nanowires have been heavily doped $n+$ after etching.
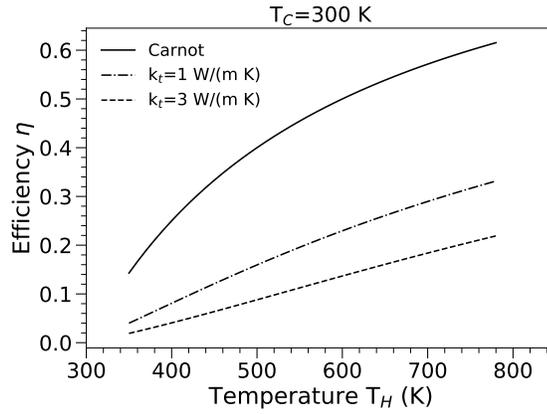

Figure 8: The efficiency of a thermoelectric generator, based on Si nanowires, is reported as a function of the hot temperature T_H. The cold temperature T_C is 300 K. As expected, the efficiency is higher for lower values of the thermal conductivity k_t. The theoretical Carnot efficiency is reported as a comparison.
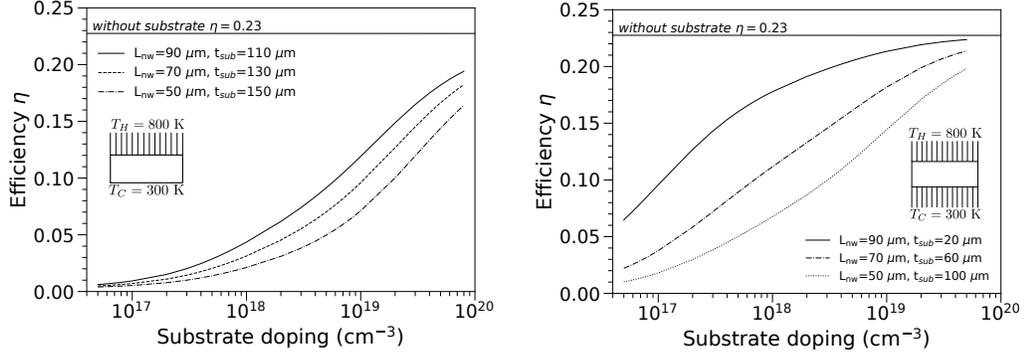
Figure 9: The maximum efficiency of a thermoelectric generator, based on Si nanowires on a single face of a silicon wafer (left panel) or on both faces (right panel), is reported as a function of the substrate doping. T_H is 800 K, T_C is 300 K. Different curves are related to different nanowire lengths. The sum of the nanowire lengths and of the substrate thickness is 200 μm. The ideal value of the efficiency achievable without the substrate is reported for comparison.
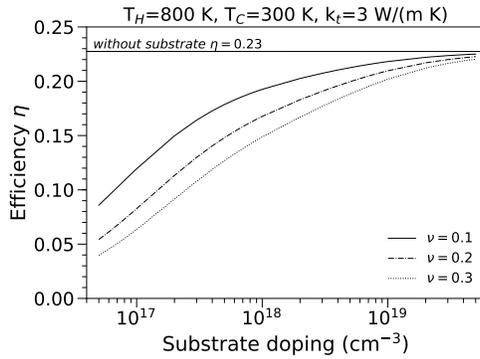

Figure 10: The efficiency of a double nanowire forest with $L_{nw} = 90$ μm and $t_{sub} = 20$ μm is reported as a function of the doping of the substrate. Different curves are related to different values of the coverage ratio ν. The temperature has been fixed at T_H of 800 K and T_C of 300 K. The ideal value of the efficiency without the substrate is also reported.

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