

Large thermal biasing of individual gated nanostructures

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We demonstrate a novel nanoheating scheme that yields very large and uniform temperature gradients up to about 1 K every 100 nm, in an architecture which is compatible with the field-effect control of the nanostructure under test. The temperature gradients demonstrated largely exceed those typically obtainable with standard resistive heaters fabricated on top of the oxide layer. The nanoheating platform is demonstrated in the specific case of a short-nanowire device.

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In the past decade much effort was directed to the investigation of the thermoelectric (TE) properties of innovative materials. Such a revival of TE science was largely driven by the interest in solid-state energy converters^{1–4} and by the development of novel advanced materials⁵ and, in particular, nanomaterials^{6–8}. Indeed, the achievement of an efficient and cost-effective TE technology depends on the optimization of a set of interdependent material parameters of the active element: the Seebeck coefficient S and the heat and charge conductivities κ and σ . Recent developments in nanoscience yielded new strategies for the design of novel and more efficient nanomaterials in which the strong interdependency between S , κ and σ can be made less stringent^{9–12}. Despite the host of available theoretical predictions^{12–16}, however, the optimization of the TE behavior of nanostructured materials still remains an open and actively investigated problem^{17,18}, in particular for what concerns the influence of electron quantum states engineering on the power factor σS^2 . This led to the development of a number of experimental arrangements designed to impose a controllable thermal bias over micrometric or even submicrometric active elements and to measure how this affects charge transport in the device. Differently from macroscopic active elements, nanoscale TE materials also allow the investigation of thermal effects in devices where field-effect can be used to control carrier density^{18,19} or even quantum states energetics^{20,21} and coupling²². While this may not be a directly scalable strategy in view of applications, it is particularly useful for what concerns the fundamental investigation of the impact of doping - a key parameter - on TE performance. Various examples of microheating systems were reported in the literature. These include (i) suspended SiN_x microheaters, which enable a precise estimate of the κ of individual nanostructures, but also pose non-trivial technical challenges^{23,24} and do not allow the field-effect control of the nanostructure behavior; (ii) resistive heaters fabricated on top of standard Si/SiO_2 substrates, which are instead typically used to estimate S and allow also the field-effect control of carrier density^{19,22,25–28}.

Here we demonstrate an innovative buried-heater (BH)

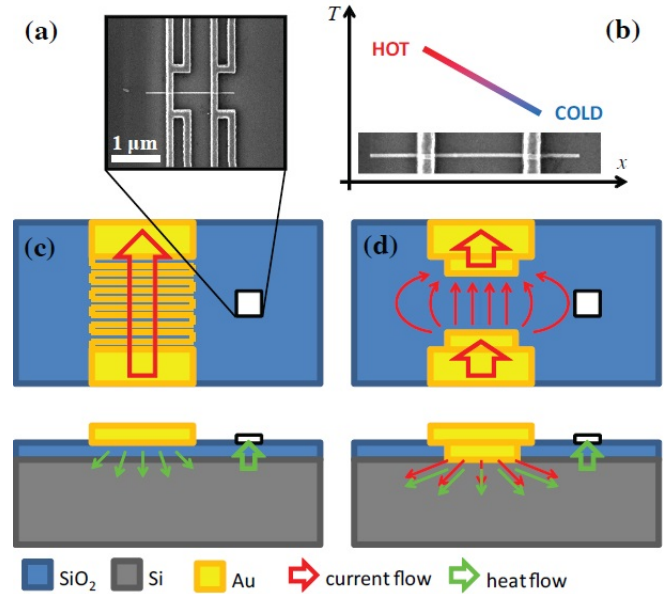


FIG. 1: The measurement of field-effect dependence of thermoelectric effects in single nanostructures (a nanowire device is visible in panel (a)) requires the application of a strong thermal gradient (panel (b)). A standard approach consists in the fabrication of a top heating element (panel (c)). An alternative “buried” architecture exploiting current flows into the bulk is visible in panel (d).

scheme based on current diffusion in the conductive bulk of a SiO_2/Si substrate. This scheme is different from the more standard one of “top” heaters (THs) relying on resistive elements microfabricated on top of the oxide layer. We shall show that our architecture yields very large and uniform thermal gradients easily exceeding $5 \text{ K}/\mu\text{m}$ and up to about $10 \text{ K}/\mu\text{m}$, far beyond typical values reported in the literature for THs. In addition, similarly to the case of TH architectures, our scheme allows the control of the nanostructure behavior by field effect. A sketch of the two alternative TH and BH schemes is visible in Fig. 1. The TH scheme relies on the diffusion of heat from a metallic resistive element through the oxide, into the sub-

strate and thus below the nanostructure. Differently, our BH approach exploits a direct differential Joule heating below the nanostructure position and bypasses the conductive bottleneck represented by the oxide between the heater and the substrate. As a consequence, our heating scheme largely outperforms TH performance reported so far in the literature and opens new possibilities for the investigation of TE effects on individual nanoscale active elements. In addition, a careful design of the current-injection electrodes allows us to obtain a strong thermal gradient and to retain a controllable gating despite the presence of an electric field in the substrate. It is also crucial to note that in both cases heaters can be fabricated in any position and orientation on a Si/SiO₂ substrate and they are thus applicable to the investigation of the effect of a thermal bias on nanostructures which are transferred by drop casting or similar methods, i.e. typically with a random position and orientation.

The article is organized as follows: in Sec. I we describe the fabrication procedure and discuss our BH design, also based on finite-element simulations; in Sec. II we describe the operation of the heater and report its performance using resistive thermometers patterned on top of the Si/SiO₂ substrate; in Sec. III we discuss heater performance and compare an experimental Raman mapping of the SiO₂ temperature with a detailed simulation. In Sec. IV, the operation of the nanoheater is demonstrated on a single-nanowire field-effect transistor (FET) with a channel length of 1 μm .

I. HEATER DESIGN AND FABRICATION

Heaters were built starting from a highly-conductive ($\rho = 0.001 - 0.005 \Omega\text{cm}$) Si substrate coated with a 280 nm-thick oxide layer. The injection electrodes consist of two $1 \times 10 \mu\text{m}^2$ windows in the oxide, separated by 9 μm . These were defined by e-beam lithography using PMMA resist and etched in a buffer-oxide etch solution for 5 min. Immediately after etching a Ni/Au bilayer (10/25 nm) was deposited to contact the Si substrate. These contacts were connected to the large bonding pads using a wide and thicker Ti/Au (10/100 nm) evaporation step. It is important to note that the heater can be freely placed anywhere on the Si/SiO₂/ substrate and thus be aligned, for instance, to an existing nanostructure deposited on the oxide surface. However, the need to preserve the integrity of the nanostructures poses non-trivial constraints on the processing steps; for example, standard rapid thermal annealing of the heater contacts is not always possible. The device structure can be seen in the scanning electron micrograph and sketch of Fig. 2a and 2b. Further details of the contact region are visible in the tilted image of Fig. 2c and in the cross-section sketch of Fig. 2d. As visible in Fig. 2a, sets of four-wire resistive thermometers were fabricated together with the Ti/Au connection layer and later used to monitor the local temperature on the surface of the substrate.

The contact geometry visible in Fig. 2b was designed in order to achieve: (i) a large and uniform thermal bias at a position which is relatively far from the injection contacts; (ii) minimal non-uniformity in the electrostatic potential below the nanostructure under study in the presence of a heating current. A two-contact design was chosen because it allows to achieve a virtually vanishing voltage drop on the symmetry plane between the injection electrodes $H\pm$ when an asymmetric heater bias $V_{H\pm} = \pm V_H$ is applied. The ratio between the contact size L and respective distance W was decided based on finite-element simulations indicating that the most uniform gradient is obtained for $W \approx L$. Calculation parameters and boundary conditions are discussed in further detail in the Supplementary Information while results are sketched in Fig. 3. The overall size of the heater was decided based on the length of the studied nanowire structures, which is of the order of one to few microns. Particular care was also taken in placing thermometer leads approximately along the expected heater constant-temperature lines, in order to avoid unwanted heat flow along the leads' and thermometers' electrodes.

II. HEATER OPERATION

The as-fabricated BH typically displays highly non-linear transport characteristics, as visible from curves in Fig. 4a. This is not surprising since the Ni/Au contacts on Si are known to display a Schottky behavior when no thermal treatment is performed and the semiconductor is

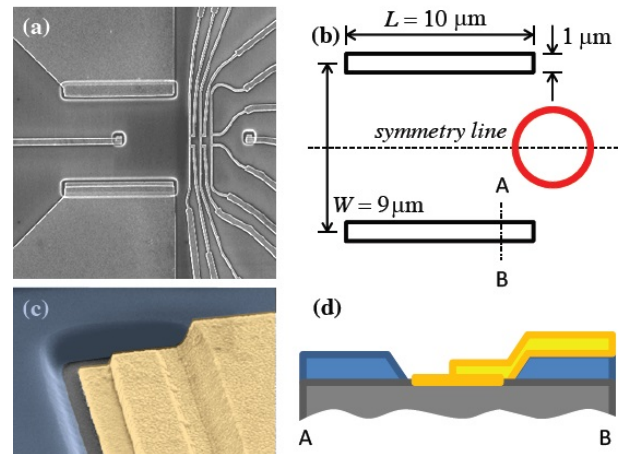


FIG. 2: (a) Scanning electron micrograph of one of the fabricated buried heaters. (b) Sketch of the contact geometry: the heater is designed to achieve the best differential heating conditions in the red circle area, which is the one where the nanostructure is supposed to reside. (c) Blow-up image of one of the current injection contacts used to feed current to the substrate through a hole in the 280 nm-oxide covering the Si substrate (sample was tilted by 60 degrees). (d) Cross-section sketch of the contact region.

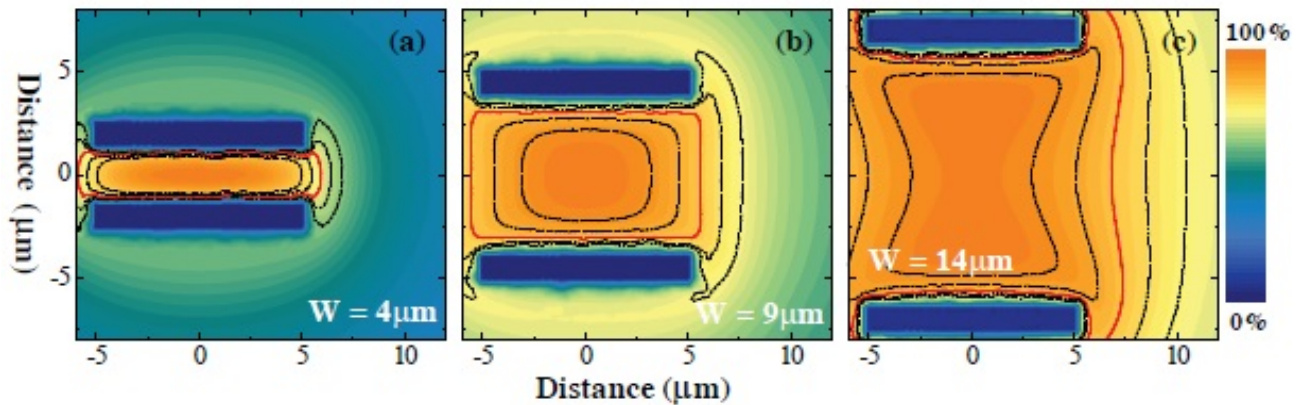


FIG. 3: Finite element estimate of the temperature profiles for different values of the L/W ratio in the studied geometry and assuming an ideal thermal sinking at the heater contacts for sake of simplicity. The colorplot reports the temperature increase ΔT as a per cent of the maximum value in the heated regions. For a fixed $L = 10 \mu\text{m}$ the (a), (b) and (c) panels report the case $W = 4, 9$ and $14 \mu\text{m}$, respectively. The red contour lines corresponds to the highest gradient along the symmetry line of the heater while the dashed lines are spaced by 5% of the top ΔT . An optimal uniformity at the top gradient position is achieved for $H \approx L$.

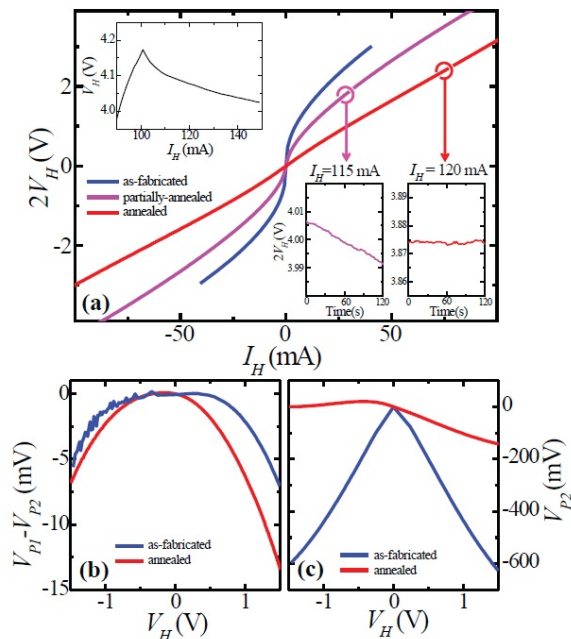


FIG. 4: (a) IV characteristics of the heater before (blue), during (magenta) and after (red) the self-annealing procedure. Top inset: a high driving current can lead to a time-dependent evolution of the IV. Bottom insets: the drift of the heater voltage V_H at fixed I_H and as a function of time. (b,c) Voltage difference between the two substrate probes $V_{P1}-V_{P2}$ and individual value of V_{P2} . Both panels report the characteristics at various stages of the self-annealing procedure, according to the plot color.

not very strongly doped. Such non-ideal behavior of the

BH contacts can be detrimental since it leads to an uneven heating caused by the voltage-drop occurring at the contact position. In addition, non-ohmic contacts can cause a significant deviation from device symmetry under bias and, as a consequence, the back-gate voltage at the nanostructure position can become difficult to predict and control. Since the heater is meant to be fabricated on a SiO_2/Si substrate already hosting the nanostructures to be studied, we developed a procedure for ohmic-contact formation which avoids possibly dangerous standard annealing protocols. Indeed, a *self-annealing* procedure was performed exploiting the fact that a significant part of the injected power will be dissipated at the reverse-biased Schottky contact. The blue curve in Fig. 4a represents an example of a typical IV curve of a BH before the self-annealing step. The heater was first biased using a current I_H , corresponding to a voltage drop defined as $2V_H$, consistently with the asymmetric voltage bias procedure that we will use in the following part of our analysis and with the notation of our previous work²⁸. Contact quality was improved by successive back and forth sweeps of the BH current I_H between $-I_0$ and $+I_0$ for increasing values of I_0 . The procedure was performed at room temperature. As visible in the top-left inset of Fig. 4a, when sufficiently high currents are driven into the BH, heat dissipation at the reverse-biased contact starts to modify the contact properties and the IV curve displays a strong non-linear evolution due to its time-dependent shift to lower resistance values. This leads to a drop in the heater voltage $2V_H$ even while I_H values keep increasing. It is important to stress that the process was repeated for both current directions in order to achieve good annealing for both contacts. The sweeps were repeated until no significant evolution was observed for a given I_0 value. Once the IVs became stable, I_0 was stepped to higher

values. The process was repeated in small steps in order to avoid damaging the heater contacts and up to a top current $I_0 = 150$ mA. The pink curve in Fig. 4a results from a partial self-annealing while the red curve corresponds to a fully self-annealed BH. The corresponding time drifts of the heater voltage $2V_H$ as a function of time and at a fixed bias current I_H are shown in the bottom-right inset, with matching colors. In the case of the fully self-annealed BH, no drift is observed even at a significant current bias of 120 mA.

As mentioned before, the Si substrate of the BH can also be used as a backgate to control the nanostructure properties by field effect. This can be achieved by applying a bias voltage $V_{H\pm} = V_{bg} \pm V_H$ to the two BH leads. In a perfectly symmetric device this would lead to a gate voltage V_{bg} at the nanostructure position. However, given the residual asymmetry of the heater contacts, a direct measurement of the Si-bias value at the nanostructure position was carried out. Since it is not possible to contact the Si directly below the nanostructure, the Si potential was probed at the two ends of the nanostructure (V_{P1} and V_{P2} , see Fig. 2a). The values measured at the two probes are typically very consistent, with small deviations of few millivolts even at the highest V_H values and both before and after the self-annealing procedure (see Fig. 4b). Such a small difference indicates that biasing is uniform along the symmetry line of the BH, in the nanostructure region. The importance of the self-annealing procedure is also evident from curves in Fig. 4c, where we report the absolute value of V_{P1} for $V_{bg} = 0$ and as a function of V_H . Before the annealing (blue curve), V_{P1} can be a significant fraction of the applied V_H , consistently with the presence of two Schottky contacts. The situation is much improved after the annealing process (red curve) and the observed values are much closer to the ideal case $V_{P1} = V_{bg} = 0$.

III. THERMAL PERFORMANCE

Figure 5 illustrates the thermal characteristics of the BH in operation. The two-dimensional heating profile was directly mapped by means of a micro-Raman technique which exploits the temperature dependence²⁹ of the Raman shift of the Si band at 520 cm^{-1} . The sample was mounted on a three-axis piezo translator allowing precise positioning and electrical access to the heater. The sample was illuminated through a 100X objective with a numerical aperture of 0.7 with the 488-nm line of an Argon laser. The laser power on the sample was kept low (1mW) to avoid heating effects. Spectra were obtained by dispersing the scattered light with a 550-mm-focal-length spectrograph and focused onto a thermoelectrically cooled CCD. A full spectrum was acquired for each pixel of the map and post-processed by fitting the main Si peak with a Lorentzian curve to determine the precise position (ω) of the band. The corresponding temperature was calculated as $T = T_0 - (\omega - \omega_0) \times$

$0.022 \text{ cm}^{-1}/^\circ\text{C}$, where T_0 is the temperature of the device without any applied power (measured with a thermometer in close proximity to the μ -Raman system) and ω_0 the Raman shift of Si at T_0 .

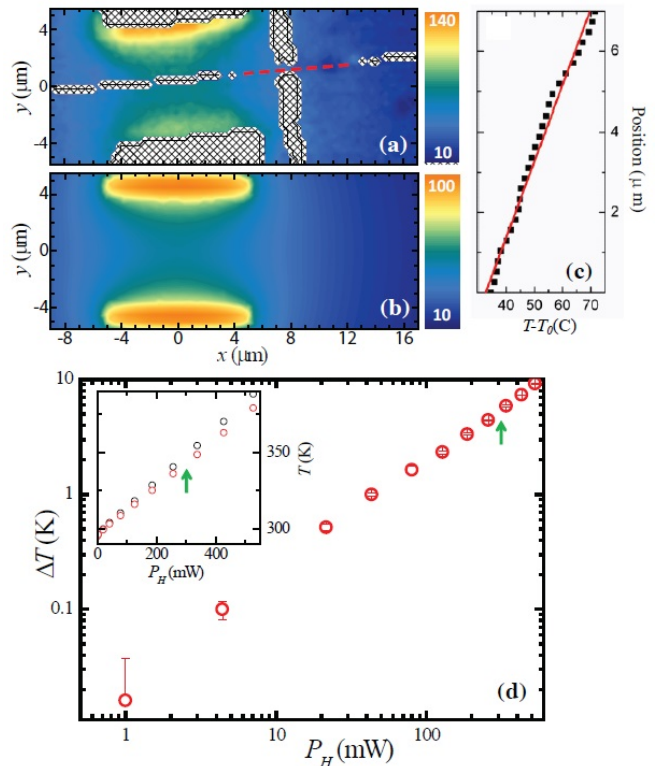


FIG. 5: (a) Raman map of the local temperature increase of the SiO_2/Si substrate in the vicinity of the heater and of the device measurement site. (b) Numerical simulation for a injected power of about 300 mW including the lead finite heat conductivity and contact dissipation. (c) The measured temperature profile along the red dashed line on the Raman map. (d) Temperature difference between two resistive thermometers spaced $1 \mu\text{m}$ (see Fig. 2a) as a function of the electrical power fed heater. The green arrows highlight the power used for the Raman map.

The heating profile $T - T_0$ is shown in Fig. 5(a) for a biasing condition $V_H = 1.6$ V and $I_H = 95$ mA, corresponding to a total injected power $P_H = 304$ mW. Hatched areas correspond to metal-covered areas of the device where the Si Raman signal could not be detected. The measured profile indicates that contacts get significantly hotter with respect to the ideal case shown in Fig. 3, indicating that an important effect is played by the non-perfect thermal sinking of the injection contacts as well as, most probably, by the local resistive heating at the metal-semiconductor interface. Figure 5(b) reports the result of a more refined numerical simulation including contact leads and an interface resistance at the electrode-Si contact. The resulting heating profile was calculated for a power dissipation of about 300 mW

within the substrate and the heater contacts. A closer match to the actually observed T profile is obtained and the overall heater behavior matches our expectations. In particular, the observed behavior confirms that a large and uniform gradient can be obtained with the chosen contact geometry. Further details about the numerical calculations are reported in the Supplementary material. A profile of the experimental temperature along the white dashed line shown in Fig. 5a is reported in Fig. 5c. The gradient was determined to correspond to $5.3 \pm 0.2 \text{ K}/\mu\text{m}$ by linearly fitting the data (red line in the plot).

The effective BH performance was also cross-checked using a set of resistive thermometers, as also visible in the right side of the heater in Fig. 2a: these measurements were found to be consistent with Raman data. In Fig. 5d we report the temperature difference between two thermometers spaced by $1 \mu\text{m}$. The temperature gradient was found to grow linearly with the power applied to the heater. In the device shown, a difference of almost 10 K was obtained by feeding about 500 mW into the BH circuit. Correspondingly, the absolute temperature of the thermometers - and thus that of the nanostructure - increased on average by less than 100°C (see inset). The green arrows highlight the power setting used during the measurement of the Raman map of Fig. 5a. Linear interpolation of the available data yields $\Delta T(P_H = 304 \text{ mW}) = 5.29 \text{ K}$, and thermometer temperatures $T_1 = 347.98 \text{ K}$ and $T_2 = 342.69 \text{ K}$. These absolute values are consistent with the data that can be deduced from the Raman map.

IV. THERMOVOLTAGE ON SINGLE NANOSTRUCTURES

The above-described differential heating architecture was directly tested on a relatively-short InAs-nanowire FET with a channel length of $1 \mu\text{m}$, as visible in the scanning electron micrograph of Fig. 6a. The device was fabricated starting by drop-casting n-doped InAs nanowires on top of the SiO_2/Si substrate pre-patterned with a set of markers. The nanowire position was then determined with respect to the markers. Heater and contacts were fabricated aligned to the randomly-deposited nanostructure. The contact leads of the nanowire were designed to work also as resistive thermometers and were obtained by a Ti/Au evaporation (10/100 nm). Prior to the contact deposition, wires were passivated by an ammonium sulfide solution in order to remove the native oxide on the InAs surface and promote contact formation. A blow-up of the device active region is visible in Fig. 6b: note that it is located in front of the heater structure.

The application of controlled, strong thermal gradients is crucial for the investigation of thermoelectric effects on single micrometric or even submicrometric nanostructured materials. Figure 6c shows the result of a set of measurements of the Seebeck coefficient of single nanowires as a function of the field-effect-controlled car-

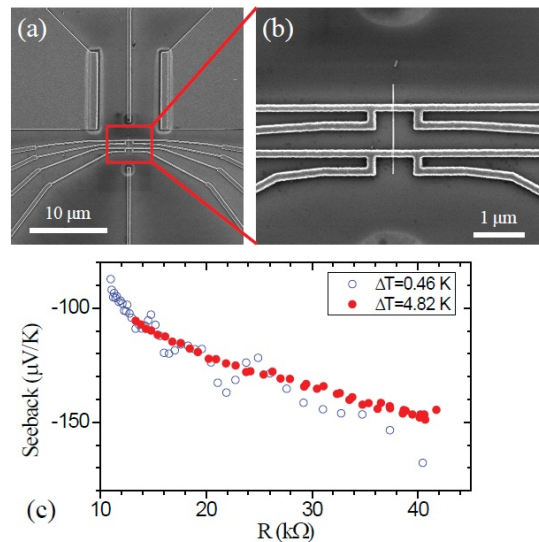


FIG. 6: (a) Scanning electron micrograph of the studied nanowire device and (b) blow-up of the isolated nanostructure. (c) Measurement of the field-effect evolution of the Seebeck coefficient plotted parametrically against the nanowire resistance. The application of a strong gradient of $\approx 5 \text{ K}/\mu\text{m}$ allows to obtain a much clearer evidence of the effect.

rier density. The resistance of the wire changes with the carrier density and is used as the abscissa in the parametric plot. Measurements were performed at room temperature. The advantage of the large gradient is evident by comparing the two curves obtained for a thermal bias ΔT of 0.46 K and 4.82 K. While the two data are consistent, the large ΔT dataset is much cleaner since S is calculated as the ratio of the thermovoltage and ΔT and its error obviously scales as $1/\Delta T$ for a given measurement protocol.

V. CONCLUSIONS

We demonstrated a BH architecture which makes it possible to reach a thermal gradient of almost $10 \text{ K}/\mu\text{m}$ with an overall temperature increase of few tens of degrees with respect to the bath temperature at the nanostructure position. This result was obtained using the substrate as the active heating element and thus exploiting non-uniform Joule heating effects and bypassing the thermal impedance of the oxide layer. This scheme outperforms results reported in the literature and based on a TH approach: these are typically limited to gradients of fractions of $\text{K}/\mu\text{m}$ ^{19,25,27}. The differential heating architecture presented here was demonstrated on a single-nanowire device with an active channel of $1 \mu\text{m}$. The possibility to achieve a gradient of this magnitude can significantly enhance the visibility of thermoelectric effects on the micrometer scale and reduce measurement errors, enabling the investigation of even smaller nano-

metric active elements.

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