

A chopper instrumentation amplifier with input resistance boosting by means of Synchronous Dynamic Element Matching

F. Butti, M. Piotto, P. Bruschi

Abstract—In this work, we propose a method to increase the parasitic input resistance caused by application of chopper modulation to indirect current feedback instrumentation amplifiers. The result is obtained by applying dynamic element matching to the input and feedback ports at the same frequency as chopper modulation. The proposed approach requires effective offset ripple rejection and equalization of the input and feedback common mode voltages. An in-amp architecture that meets both requirements and embodies the proposed input resistance boosting method is described. Experimental verification is provided by means of a prototype designed and fabricated using the 0.32 μm CMOS devices of the STMicroelectronics BCD6s process. The amplifier operates with a 3.3 V supply voltage and a total current absorption of 170 μA . An input impedance in excess of 1 G Ω has been measured at a chopper frequency of 20 kHz. The input referred voltage noise density is 18 nV/sqrt(Hz) with a flicker corner of 0.2 Hz and 200 Hz bandwidth.

Index Terms—Instrumentation Amplifier, Input Resistance, Chopper Amplifier, Current Feedback.

I. INTRODUCTION

INSTRUMENTATION amplifiers (in-amps) represent the ideal solution for interfacing sensors whose output signal is a differential voltage [1]. The continuous progress in the field of integrated sensors and the growing interest in fully integrated systems for bio-potential monitoring are motivating the design of new in-amps [2-7], with particular emphasis on reduced area, low power consumption and high common mode rejection ratio (CMRR). In most cases, the signal bandwidth extends to very low frequencies or even includes DC. In CMOS circuits, this dictates the adoption of dynamic approaches to cancel the input offset voltage and reduce flicker noise [8,9]. Among these techniques, chopper modulation, being immune to noise fold-over, represents an optimal choice in terms of power consumption vs noise tradeoff. A very popular architecture is the indirect current

feedback (ICF) in-amp [10], which reaches high CMRR's with no need of resistor trimming and can accomplish chopper modulation with minimal changes [11,12].

A weakness of ICF in-amps with respect to their voltage feedback counterpart is that the input resistance is not increased by feedback. This is a serious drawback when combined with chopper modulation, which introduces a parasitic switched-capacitor resistance across the input terminals. This resistance is due to the periodic charging and discharging of the input capacitance caused by the input modulator [13]. With typical input capacitance values and chopper frequencies, the parasitic resistance can fall below 1 M Ω . Considering that the output resistance of integrated sensors (e.g. thermoelectric micro-transducers) may be of the order of several tens of k Ω , the resulting input attenuation significantly degrades gain accuracy. As it will be explained in next section, compensation of the input attenuation during the sensor calibration phase may be a non-optimal solution.

In this work, we propose a method to increase the input impedance of ICF chopper instrumentation amplifiers by simply using a Dynamic Element Matching (DEM) approach, consisting of periodically swapping the input and feedback signals at the transistor inputs (port swapping). A similar technique was originally proposed as a solution for the gain error caused by input transistor mismatch [14]. However, in earlier implementations, the DEM frequency was a submultiple of the chopper frequency. As it will be shown in next section, a large increase of the input impedance can be achieved only if DEM and chopping are synchronous (SCPS: synchronous chopping and port swapping). For this method to be applicable, the output voltage should be free from ripple; furthermore, the common mode voltages of the input and feedback signals should be as close as possible. To reject all contributions to the output ripple, an amplifier with a second order low pass frequency response has been designed [15, 16], while the input and feedback common mode voltages are equalized by means of a closed loop approach [17]. So far, experimental demonstration of the mentioned techniques was not provided yet. In addition, the input impedance boosting effect of SCPS is described in this paper for the first time.

Experimental validation of the proposed ideas is provided by means of detailed measurements performed on a prototype designed using the 0.32 μm , 3.3 V CMOS devices of the STMicroelectronics process BCD6s (Bipolar-CMOS-DMOS).

Submitted on July 28, 2016. Revised version submitted on Oct. 28, 2016

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II. PRINCIPLE OF OPERATION

A. Standard ICF topology with chopper modulation

A typical fully differential chopper stabilized ICF in-amp is shown in Fig.1. Switch matrices S_{in} , S_{fb} and S_o , controlled by the clock signal ck (frequency f_{ck} , 50 % duty-cycle), transmit the signal through the solid lines when $ck=1$ and through the dashed ones when $ck=0$. The input, feedback and output signals are characterized by v_{in} , v_{fb} and v_{out} differential mode voltages and V_{CMI} , V_{CMF} and V_{CMO} common mode voltages, respectively.

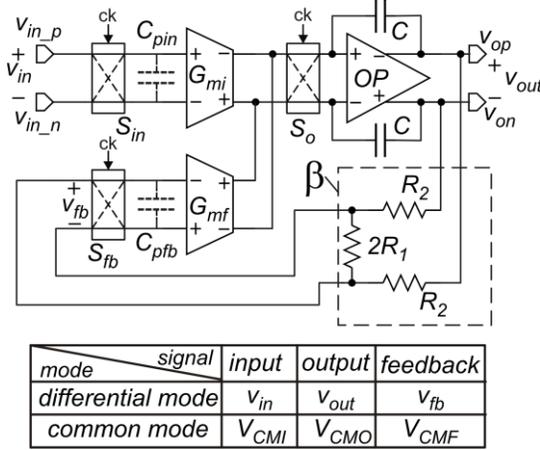


Fig.1. Standard indirect current feedback (ICF) architecture. The table on the bottom introduces the signal definitions used throughout the paper.

Block β is a resistive voltage divider such that $v_{fb} = \beta v_{out}$, with $\beta = R_1 / (R_1 + R_2)$, while with G_{mi} and G_{mf} we indicate both the input transconductors and their transconductances, defined as the ratio of the output differential current over the input differential voltage. The input differential capacitances of G_{mi} and G_{mf} are C_{pin} and C_{pfb} , respectively. Amplifier OP and capacitors C form a Miller integrator.

Keeping ck fixed to a constant logic value (clock turned off), the circuit in Fig.1 behaves like a first order low pass filter with cut-off frequency:

$$f_c = \frac{1}{2\pi} \frac{\beta G_{mf}}{C} \quad (1)$$

If the DC loop gain of the circuit is much greater than one, then the DC closed loop gain of the ICF in-amp can be approximated by:

$$A = \frac{G_{mi}}{G_{mf}} \frac{1}{\beta} \quad (2)$$

Since, by design, $G_{mi} = G_{mf}$, the nominal gain is $1/\beta$. When the clock is activated, v_{in} and v_{fb} are modulated by S_{in} and S_{fb} and demodulated by S_o , resulting virtually unchanged, while the output offset and flicker noise of G_{mi} and G_{mf} are processed only by S_o , which shifts them to higher frequencies where they can be removed by a low pass filter (not shown in Fig.1). In particular, modulation of the offset voltage produces a periodic waveform with frequency f_{ch} (offset ripple), which

is difficult to reject with fully integrated filters and represents one of the most serious drawback of the chopper modulation approach.

The chopper frequency is the result of several trade-offs: high chopper frequencies improve flicker noise rejection and allow for wider amplifier bandwidth; whereas low chopper frequencies reduce power consumption and result in lower residual offset [8]. Optimal chopper frequencies for low offset in-amps are of the order of a few tens of kHz.

As far as the parasitic input resistance [13] is concerned, the mechanism involved is illustrated in Fig.2 where the input part of the circuit in Fig.1 is represented, assuming $C_{pin} = C_{pfb} = C_p$. At each clock transition, the input differential capacitance undergoes a total voltage variation equal to $2v_{in}$, so that the charge drawn from the input source is $2C_p v_{in}$. Considering that identical charge transfers occur at the two opposite clock transitions, the equivalent input resistance is given by:

$$R_{in-chop} = \frac{1}{4 f_{ch} C_p} \quad (3)$$

The input resistance forms a voltage divider with the output resistance of the signal source, introducing an unwanted attenuation that degrades the amplifier gain accuracy.

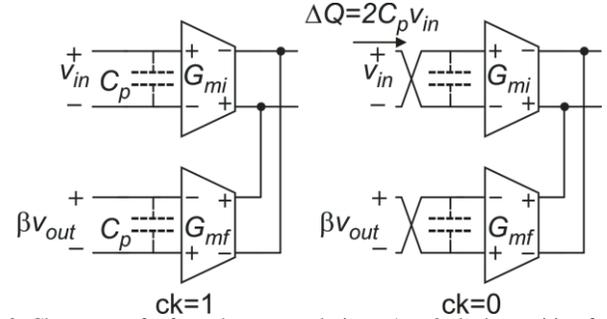


Fig.2. Charge transfer from the v_{in} port during a 1-to-0 clock transition for the traditional chopper configuration. The same charge transfer occurs during the opposite clock transition.

In principle, the input resistance given by (3) can be increased by reducing either the chopper frequency or the input device area (i.e. C_p). Unfortunately, this increases the flicker noise contribution to the residual noise in the baseband. In fact, the maximum tolerable input attenuation sets a lower limit to the achievable noise figure [18]. The noise flicker coefficients of a typical CMOS process are such that, for a given sensor output resistance, it is possible to size the $C_p f_{ch}$ product in order to obtain, at the same time, an input noise density comparable to the thermal noise of the sensor and an input attenuation of a few percent. This allows compensation of the input attenuation during sensor calibration with negligible resolution loss. Such an operation is less effective when the in-amp is included in a versatile sensor interface that has to provide optimal performances with sensor output resistances spread over an interval of more than a decade. In this case, the risk is to have too much noise at the lower end of the resistance interval or too much attenuation at the higher end. Possible dependence of sensor output resistance on temperature can also make calibration critical.

B. Proposed input resistance boosting technique

Fig. 3 shows the proposed input switching mechanism (SCPS). At the one-to-zero clock transition, the signals v_{in} and $v_{fb} = \beta V_{out}$ are swapped together. At the same time, the inverting and non-inverting terminals are also swapped, producing chopper modulation of both signals. For the sake of simplicity, let us consider that both v_{in} and v_{out} are constant signals. Then, at any clock transition, the charge sourced by v_{in} is equal to $C_p(v_{in} - \beta v_{out})$. In an ideal ICF amplifier (infinite DC loop gain), $v_{out} = v_{in}/\beta$, so that charge transfer is zero and the input resistance is infinite.

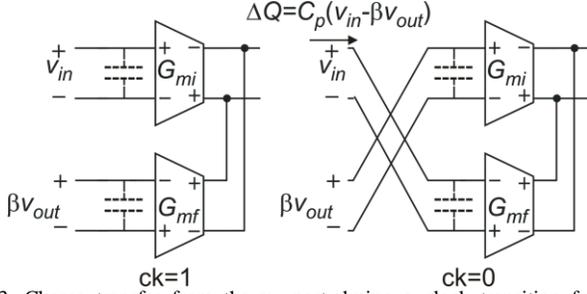


Fig.3. Charge transfer from the v_{in} port during a clock transition for the proposed approach.

The analysis can be easily extended to non-DC input signal, provided that the spectrum of v_{in} is confined to frequencies much lower than f_{ch} , so that we can still consider v_{in} and v_{out} to be constant across a clock period. In these conditions, charge transfer over a clock period is $2C_p(v_{in} - \beta v_{out})$. Indicating the amplifier closed-loop frequency response with $H(f)$, the average current in a clock period becomes: $2C_p v_{in} [1 - \beta H(f)]$. Hence, the input impedance is given by:

$$Z_{in}(f) = \frac{1}{2[1 - \beta H(f)]f_{ch} C_p} \quad (4)$$

Comparing this expression with (3), it is apparent that the impedance boosting is effective for signals well within the amplifier bandwidth, where $\beta H(f)$ is close to one, while the actual advantage gradually decrease as the amplifier cut-off frequency is approached.

Note that swapping the input and feedback signals is equivalent to swapping the input transconductors, similarly to the DEM technique proposed in [14-16] as a method to reduce the impact of G_{mi}/G_{mf} mismatch on the gain accuracy. However, if f_{DEM} is a submultiple of the f_{ch} (e.g. $f_{dem} = f_{ch}/4$ in [14]) part of the chopper transitions are still accomplished by simply inverting the connections on the input and feedback capacitance, just as shown in Fig.2. These chopper transitions, which are not accompanied by a DEM swap, still draw a full charge packet equal to $2v_{in}C_p$. The only effect is reducing the frequency by which full charge packets are drawn. For example, with $f_{dem} = f_{ch}/2$ the input resistance is only doubled. With lower f_{dem}/f_{ch} ratios, as in [14], the effects are even smaller. It is then apparent that the condition to obtain a much larger input resistance-boosting factor is combining each chopper transition to a DEM transition, i.e. f_{DEM} should be equal to f_{ch} .

Application of the impedance boosting approach requires that two conditions are fulfilled: (i) the ripple superimposed on v_{out} is negligible; (ii) input and feedback common mode voltages coincide.

Ripple is reflected in the feedback signal, degrading v_{in} vs v_{fb} matching, hence reducing the effectiveness of the impedance boosting mechanism. Rejection of the output ripple by simply cascading an active filter is likely to introduce significant offset and flicker noise contributions, unless the filter occupies much more area than the amplifier, or off-chip capacitors are used [19]. Feedback loops requiring demodulation of the individual ripple components have been demonstrated to be very effective [20-22]. Other solutions that make use of switched capacitor filters [23, 24] to reject the offset ripple require sampling of the amplifier output voltage and, consequently, introduce noise fold-over. Combinations of auto-zero and chopper techniques, implemented with a ping-pong architecture [25], are much less prone to offset ripple artifacts, but are less effective in terms of power consumption and compactness. Digital trimming of the input pair can be used when the focus is on compactness and less effective ripple rejection is tolerable [26]. In this work, ripple rejection was accomplished by embedding a second order low-pass filtering function into the amplifier [15,16].

As far as the effect of input common mode voltage mismatch is concerned, Fig.4 illustrates the phenomena involved. First, at each DEM transition, the common mode components of the input capacitances, indicated with C_{cm} in Fig. 4(a), experience a voltage variation just equal to $V_{CMI} - V_{CMF}$. As a result, an input bias current equal to $2C_{cm}f_{DEM}(V_{CMI} - V_{CMF})$ is drawn from the input source. Second, input common mode alternation caused by port swapping alters the operating point of the input transconductors. Let us consider the case of an n -type input pair, as shown in Fig.4(b) and suppose, for simplicity, that the input differential voltage is very small, so that $V_{GS1} \sim V_{GS2}$.

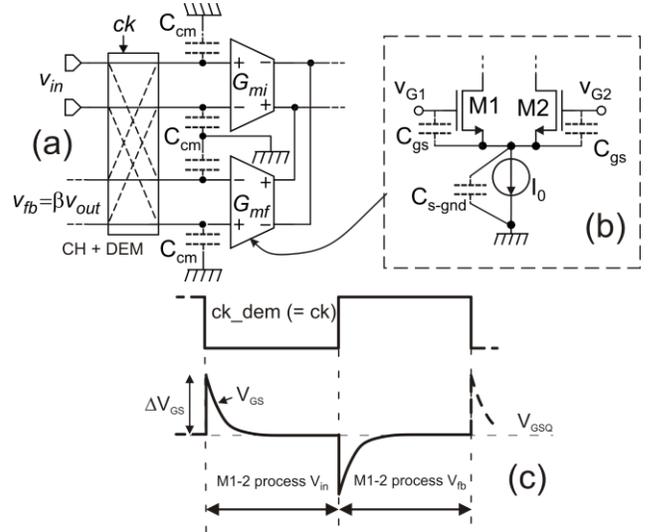


Fig.4 Effects caused by application of DEM when the input and feedback common mode voltages are different. (a) Input transconductors with common mode capacitances C_{cm} ; (b) input differential pair with relevant capacitances; (c) variation of M1-2 V_{gs} mean value across a DEM period.

At any DEM transition, V_{GS1} and V_{GS2} undergo a variation with respect to their rest value (V_{GSQ}), given by:

$$\Delta V_{GS} = \Delta V_{CM} \frac{2C_{GS}}{2C_{GS} + G_{S-gnd}} \quad (5)$$

where ΔV_{CM} is the difference between the input and feedback common mode voltage. The V_{GS} variation is recovered after a time that can be a significant fraction of the DEM period. Fig.4 (c) shows a sketch of a possible V_{GS} behavior in the case that $V_{CMI} > V_{CMF}$. Since the transconductance of the stage monotonically increases with V_{GS} , the input signal is processed on average by a higher transconductance than the feedback one. The opposite occurs if $V_{CMI} < V_{CMF}$. According to (2), a gain error is introduced. Due to the configuration of the resistive voltage divider universally used for the feedback path (see Fig.1), $V_{CMF} = V_{CMO}$, so that this error is tolerable only for V_{CMI} values close to V_{CMO} . For $V_{CMO} - V_{CMI}$ exceeding a few hundred mV, temporary shutdown of one of the input transconductors is likely to occur at each DEM transition, exacerbating the adverse effect on the amplifier gain.

The problems illustrated in Fig.4 have been encountered also in [14], where bootstrapping of M1 and M2 substrates to reduce the input common mode capacitances was proposed as an effective solution. In this work, we solved this issue by forcing V_{CMF} to track V_{CMI} by means of a local feedback loop, which was already proposed in [17] as a way to obtain an ICF in-amp with rail-to-rail input ranges.

III. PROPOSED AMPLIFIER ARCHITECTURE

A. Description of the architecture

The proposed amplifier, shown in Fig.5 (a), is formed by the three fully differential blocks, indicated with INT1, INT2 and FB. INT1 is a Gm-C integrator, based on the two-input-port composite transconductor OTA1. INT2 is a two-input integrator, based on a Gm-C-Opamp architecture.

Switch arrays S_{ps} , S_0 and S_{mf} are controlled by a clock signal of frequency f_{ch} and 50 % duty-cycle. Feedback block FB includes a resistive voltage divider and a “common-mode differential amplifier” (CMDA), forming a local feedback loop that causes V_{CMF} to track V_{CMI} .

The amplifier ideal behavior in terms of differential components is represented by the block diagram of Fig.5 (b). In the rest of this section, we will demonstrate this equivalence finding expressions for ω_{01} , ω_{02} and β_{eff} and introducing the main sources of non-ideality. Let us start by analyzing block FB. The CMDA produces an output voltage, V_H , given by:

$$V_H = A_{CMD}(V_{CMI} - V_{CMF}) \quad (6)$$

with $A_{CMD} \gg 1$. Nominally, $R_{1A} = R_{1B} = R_1$ and $R_{2A} = R_{2B} = R_2$. We have distinguished the upper part of the divider (R_{1A}, R_{2A}) from the lower one (R_{1B}, R_{2B}) in order to take into account an unwanted common-mode to differential-mode coupling that depends on the mismatch between the upper and lower transfer function of the divider. It is convenient to express these functions in terms of mean value β and mismatch $\Delta\beta$:

$$\frac{R_{1A}}{R_{1A} + R_{2A}} \equiv \beta + \frac{\Delta\beta}{2}; \quad \frac{R_{1B}}{R_{1B} + R_{2B}} \equiv \beta - \frac{\Delta\beta}{2} \quad (7)$$

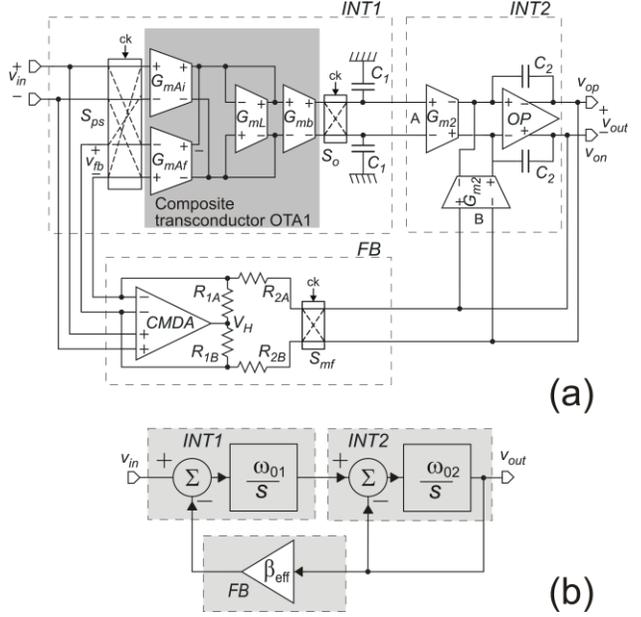


Fig.5 (a) Schematic view of the proposed architecture.(b) Ideal block diagram where differential signals are represented by a single wire for simplicity.

Considering that the effect of S_{mf} is swapping the output terminals, so that common mode components are unaffected, the following expression can be derived:

$$V_{CMF} = \beta V_{CMO} + (1 - \beta)V_H \pm \frac{\Delta\beta}{4} v_{out} \quad (8)$$

Combining (8) with (6), we get:

$$V_{CMF} = V_{CMI} \frac{(1 - \beta)A_{CMD}}{1 + (1 - \beta)A_{CMD}} + \frac{\beta V_{CMO} \pm v_{out} \Delta\beta / 4}{1 + (1 - \beta)A_{CMD}} \quad (9)$$

For $(1 - \beta)A_{CMD} \gg 1$, V_{CMF} tends to V_{CMI} , regardless of V_{CMO} and v_{out} , obtaining the desired common mode equalization.

Thus, in order to find the response of the FB block to differential signals, we can assume for simplicity that V_{CMF} is perfectly equalized to V_{CMI} , obtaining the following equation:

$$v_{fb} = \beta_{eff} v_{out} m(t) + \varepsilon_{CM} \quad (10)$$

where β_{eff} and ε_{CM} are defined as:

$$\beta_{eff} \equiv \left(1 + \frac{\Delta\beta^2}{4\beta(1 - \beta)}\right) \beta \equiv \beta; \quad \varepsilon_{CM} \equiv (V_{CMI} - V_{CMO}) \frac{\Delta\beta}{\beta} \frac{\beta}{1 - \beta} \quad (11)$$

while $m(t)$, as customary for chopper amplifiers, indicates a dimensionless unity-amplitude square waveform of frequency f_{ch} . The term ϵ_{CM} , which represents the mentioned common-mode to differential mode coupling, is an unwanted side-effect of the proposed common mode equalization mechanism. Placing modulator S_{mf} before the divider allows for simple frequency separation of the spurious term ϵ_{CM} from the useful signal ($\beta_{eff}v_{out}$), since only the latter is modulated by $m(t)$.

In order to analyze integrator INT1, it is useful to consider that composite transconductor OTA1 is equivalent to the two transconductors G_{mi} and G_{mf} of Fig.1 when the following substitutions are done:

$$G_{mi} \equiv \frac{G_{mAi}}{G_{mL}} G_{mb} ; G_{mf} \equiv \frac{G_{mAf}}{G_{mL}} G_{mb} \quad (12)$$

Note that transconductors G_{mAi} and G_{mAf} , loaded by G_{mL} act as a two-port pre-amplifier for G_{mb} . By design, G_{mAi} and G_{mAf} are identical. Indicating their nominal value with G_{mA} the pre-amplification factor is G_{mA}/G_{mL} .

Switch array S_{ps} produces chopper modulation and port swapping (DEM) at the same frequency $f_{ch}=f_{DEM}$. The only difference with respect to the scheme of Fig.3 is that v_{fb} is alternated with v_{in} , but not modulated, since, as explained above, the feedback signal is already modulated by S_{mf} .

Considering (10), and indicating OTA1 total output noise and offset currents with i_{on1} and i_{os1} , respectively, the differential mode current at the output of S_0 can be written as:

$$i_{o1} = \begin{cases} G_{mi}v_{in} - G_{mf}(\beta_{eff}v_{out} + \epsilon_{CM}) + i_{os1} + i_{on1} & \text{for } ck = 1 \\ G_{mf}v_{in} - G_{mi}(\beta_{eff}v_{out} - \epsilon_{CM}) - i_{os1} - i_{on1} & \text{for } ck = 0 \end{cases} \quad (13)$$

Defining G_{m1} and ΔG_{m1} as:

$$G_{m1} \equiv \frac{G_{mi} + G_{mf}}{2} ; \Delta G_{m1} \equiv G_{mi} - G_{mf} ; \quad (14)$$

the output current i_{o1} can be rewritten as

$$i_{o1} = G_{m1}[(v_{in} - \beta_{eff}v_{out} + v_{d1B}) + v_{d1C}m(t)] \quad (15)$$

where the baseband and modulated error sources, v_{d1B} and v_{d1C} , respectively, are defined as:

$$v_{d1B} \equiv \epsilon_{CM} \frac{\Delta G_{m1}}{2G_{m1}} \quad (16)$$

$$v_{d1C} \equiv \frac{\Delta G_{m1}}{2G_{m1}}(v_{in} + \beta_{eff}v_{out}) - \epsilon_{CM} + v_{i_{o1}} + v_{n1} \quad (17)$$

where $v_{n1}=i_{on1}/G_{m1}$ and $v_{i_{o1}}=i_{os1}/G_{m1}$ are the OTA1 input referred noise and offset voltages.

Neglecting the error sources v_{d1B} and v_{d1C} in (15), and considering that INT2 is a standard, two inputs, fully differential Gm-Op-amp integrator, it can be easily shown that

the ideal block diagram of Fig.5 (b) actually represents the amplifier differential mode response when the following expressions are used for the unity gain angular frequencies of the integrators:

$$\omega_{01} = \frac{G_{m1}}{C_1} ; \omega_{02} = \frac{G_{m2}}{C_2} \quad (18)$$

Considering also error sources v_{d1B} and v_{d1C} , given by (16) and (17), and indicating with v_{n2} , the sum of INT2 input-referred noise and offset voltages, the block diagram of Fig.6 can be easily derived from the ideal system of Fig.5 (b).

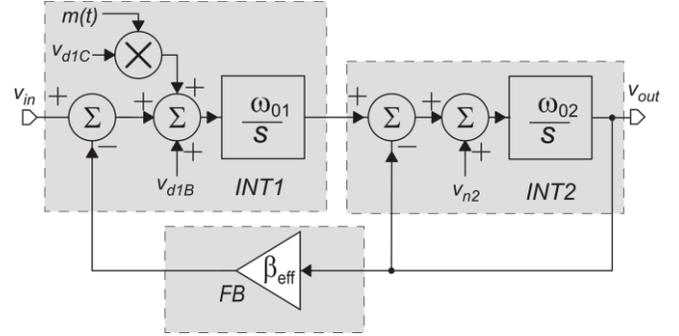


Fig.6. Block diagram representation of the proposed in-amp with main error sources.

The system depicted in Fig.6 implements a second order low pass filter with transfer function given by:

$$H_{LP}(s) \equiv \frac{v_{out}}{v_{in}} = \frac{A_0}{s^2 / \omega_c^2 + s / (\omega_c Q) + 1} \quad (19)$$

where the characteristic angular frequency ω_c , quality factor Q and DC gain A_0 are given by:

$$\omega_c = 2\pi f_c = \sqrt{\beta_{eff} \omega_{01} \omega_{02}} ; Q = \sqrt{\frac{\beta_{eff} \omega_{01}}{\omega_{02}}} ; A_0 = \frac{1}{\beta_{eff}} \quad (20)$$

Since a Butterworth-like response has been adopted, f_c coincides with the -3dB cut-off frequency of the amplifier. The effect of all error sources on v_{out} is represented by the following expression:

$$v_{out_d}(s) = (v_{d1B} + v_{d1C}m(t))H_{LP}(s) + v_{n2}H_{BP}(s) \quad (21)$$

where $H_{BP}(s)$, is a band pass transfer function given by

$$H_{BP}(s) = \frac{s / (\omega_c Q)}{s^2 / \omega_c^2 + s / (\omega_c Q) + 1} \quad (22)$$

Note that $|H_{BP}|$ reaches a maximum value of one at $\omega=\omega_c$, in contrast with $|H_{LP}|$ whose maximum value is A_0 . For $A_0 \gg 1$, this contributes to relax INT2 noise constraints. Furthermore, H_{BP} rejects v_{n2} DC components, making chopper modulation not necessary for INT2.

As far as INT1 is concerned, its equivalent input noise sources are processed by the overall amplifier response H_{LP} . It is possible to estimate the order of magnitude of the baseband

component v_{dIB} by using (11) and (16) with a conservative value of 10^{-2} for both $\Delta\beta/\beta$ and $\Delta G_{m1}/G_{m1}$ and assuming a nominal amplifier gain of 200 (i.e. $\beta=1/200$). The v_{dIB} value found in this way is lower than $1 \mu\text{V}$ for a $V_{CM1}-V_{CM0}$ mismatch up to 2 V, making this error source negligible for most applications.

Voltage v_{dIC} includes various components that are modulated by $m(t)$ producing different contributions. OTA1 noise voltage v_{n1} results in a flat noise density [8] roughly equal to v_{n1} spectral density at $f=f_{ch}$. This is the dominant contribution to the input noise voltage in the amplifier passband. All the other v_{dIC} components are constant (v_{io1}) or quasi-constant over a clock period, provided that the input signal is limited to frequencies much smaller than f_{ch} . Modulation of these terms by $m(t)$ is the origin of the output ripple. In particular, modulation of v_{io1} is the cause of the offset ripple while the term proportional to $\Delta G_{m1}/G_{m1}$ turns into the DEM ripple. Differently from previous works, such as [14], there is an additional ripple source (ϵ_{CM}), which is proportional to the input/output common mode mismatch through (11). To estimate the order of magnitude of total ripple amplitude, it is reasonable to assume the value 10^{-2} for all mismatch factors (e.g. $\Delta G_{m1}/G_{m1}$) and 1 mV for v_{io1} . Considering a DC gain of 200 ($\beta=0.005$), an input voltage ($v_{in} \cong \beta V_{out}$) of 10 mV and a $V_{CM1}-V_{CM0}$ mismatch of 1 V, then the input ripple amplitude is at most a few mV. Note that, differently from previous works using different DEM and chopper frequencies, all the ripple contributions mentioned above are modulated at f_{ch} .

Effective ripple rejection is obtained exploiting the second order low-pass transfer function of the amplifier. By setting f_c two decades below f_{ch} , the ripple is amplified by a factor that is 80 dB smaller than the passband gain. Referring the output ripple to the input port using the passband gain, the ripple equivalent amplitude is smaller than $1 \mu\text{V}$, which is a level comparable with amplifiers using the best ripple suppression approaches [14,20,21].

Note that, if the ripple is actually reduced to the values cited above, only the baseband components can be considered. In these conditions, (15) clearly indicates that v_{in} and the feedback component $\beta_{eff}v_{out}$ are processed by the same transconductance G_{m1} . Thanks to this property, for high enough a loop gain, $v_{in}=\beta_{eff}v_{out}$, even in the presence of G_{m1}/G_{mf} mismatch. This guarantee that the resistance boosting mechanism introduced by port swapping and described in Sect. II-b is robust against mismatch of the input transconductors.

To achieve this result with a chopper frequency around a few tens of kHz f_c should be a few hundred Hz. Using (18), (19) and (20) with feasible on-chip capacitance values for C_1 and C_2 , it can be easily shown that G_{m1} and G_{m2} should be of the order of a few $\mu\text{Siemens}$. This has a negative effect on the input equivalent noise voltage in the passband, which, as mentioned above, is dominated by OTA1 input noise density at $f=f_{ch}$. The problem arises from the relationship between the transconductance (G_m) and the input PSD (power spectral density) of the thermal noise voltage (S_{VTH}) which, for a single stage transconductor, is given by:

$$S_{VTH} = m_F \cdot 4k_B T \frac{1}{G_m} \quad (23)$$

where k_B is the Boltzmann constant, T the absolute temperature and m_F a topology dependent factor, typically greater than one [27]. With G_{m1} of the order of $1 \mu\text{S}$, the input noise density of OTA1 would exceed $100 \text{ nV}/\sqrt{\text{Hz}}$, which is too high for many sensor interfacing applications. With a single stage transconductor, noise reduction can be obtained only through a G_m increase, followed by a proportional capacitance increase (to keep ω_c constant), leading to excessive area occupation. The two-stage architecture of OTA1 shown in Fig.5 (a) allows for a better area vs noise trade-off [15]. In practice, the input noise PSD is reduced by a factor equal to the pre-amplifier gain with respect to a single stage having the same transconductance. The preamplifier adds a noise contribution that, fortunately, can be minimized with no side effects on the amplifier cut-off frequency. Notice that pre-amplification is not necessary for INT2 transconductors when $A_0 \gg 1$, due to the more relaxed noise constraints mentioned earlier.

B. Topology of the main blocks

The simplified schematic view of the input preamplifier is shown in Fig.7 (a), where the role of G_{mAi} and G_{MAf} is played by nominally identical differential pairs M1,M2 and M3,M4, respectively (input devices), while the function of G_{mL} is accomplished by the MO1, MO2 pair (load devices).

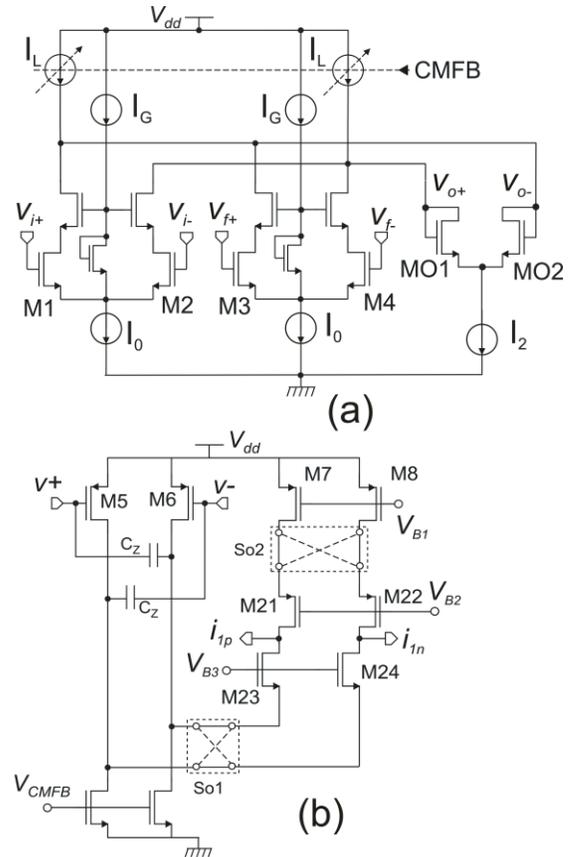


Fig.7 Elements of the OTA1 composite transconductor: (a) Schematic views of the G_{mAi} - G_{MAf} - G_{mL} preamplifier; (b) G_{mb} transconductor with embedded chopper modulator So , split into $So1$ and $So2$.

The architecture is that of a telescopic amplifier where I_L , I_0 , I_G and I_2 represent cascode current sources.

The input devices are biased in deep subthreshold to obtain the best tradeoff between input thermal noise and current consumption. On the contrary, the load devices operate in strong inversion, with an as large as possible overdrive voltage, in order to maximize the output range. As a result, the preamplifier gain is given by:

$$A_1 = \frac{g_{m-in}}{g_{m-out}} = \frac{I_0}{nV_T} \frac{(V_{GS} - V_{TH})_0}{2I_2} \quad (24)$$

where V_T is the thermal voltage ($=k_B T/q$), g_{m-in} , g_{m-out} are the transconductances of the input and load devices, respectively, $(V_{GS} - V_{TH})_0$ is the overdrive voltage of the load devices and n is the sub-threshold slope factor of the input devices.

Transconductor G_{mb} , shown in Fig. 7(b), is based on a folded cascode architecture where the voltage to current conversion is operated by the pseudo-differential pair M5-6, providing acceptable linearity over a wider input differential range with respect to conventional pairs. Capacitors C_z compensate for the positive zero due to M5-6 gate-drain capacitance, thus reducing the phase lag at the chopper frequency. The overdrive voltage of the input pair, fixed to a large value (0.72 V) to obtain a wide input range, is controlled by the preamplifier output common mode voltage. On the other hand, the overdrive voltage of the common gate devices M23-24 was set to a small value (100 mV) in order to obtain a large enough g_m . In this way, it has been possible to obtain a flat frequency response well beyond the chopper frequency. Common mode voltages of both the preamplifier and transconductor G_{mb} are stabilized by conventional CMFB circuits. Chopper modulators S_{o1} and S_{o2} perform the operation represented by S_o in Fig.5.

Fig.8 (a) shows INT2 schematic view, where the role of the two transconductors (G_{m2}) is played by M9-10 and M11-12 pairs.

The op-amp (OP in Fig.5) is implemented by the simple M13-14 pseudo differential common source stage. Considering that $I_T = 2I_B$ by design, the differential and common mode components of the transconductor output currents, indicated with I_{2n} , I_{2p} in the figure, can be approximated by the following expressions:

$$I_{2p} - I_{2n} = \frac{g_{m9}}{2} (V_{diffB} - V_{diffA}) \quad (25)$$

$$\frac{I_{2p} + I_{2n}}{2} = \frac{g_{m9}}{2} (V_{cmB} - V_{cmA}) \quad (26)$$

where $g_{m9} = g_{m10} = g_{m11} = g_{m12}$, V_{diffA} and V_{diffB} are the input differential voltages of port A and port B, respectively (see Fig.5) and V_{cmA} and V_{cmB} are their respective common mode voltages.

Due to (25), G_{m2} is given by $g_{m9}/2$. On the other hand, (26) is exploited to avoid a CMFB circuit for INT2. Considering the OP large common-mode-to-common mode gain and that,

due to feedback connection of Fig.5, V_{cmB} is equal to V_{CMO} , the latter simply tracks V_{cmA} , which is stabilized by the CMFB circuit of the previous block (INT1).

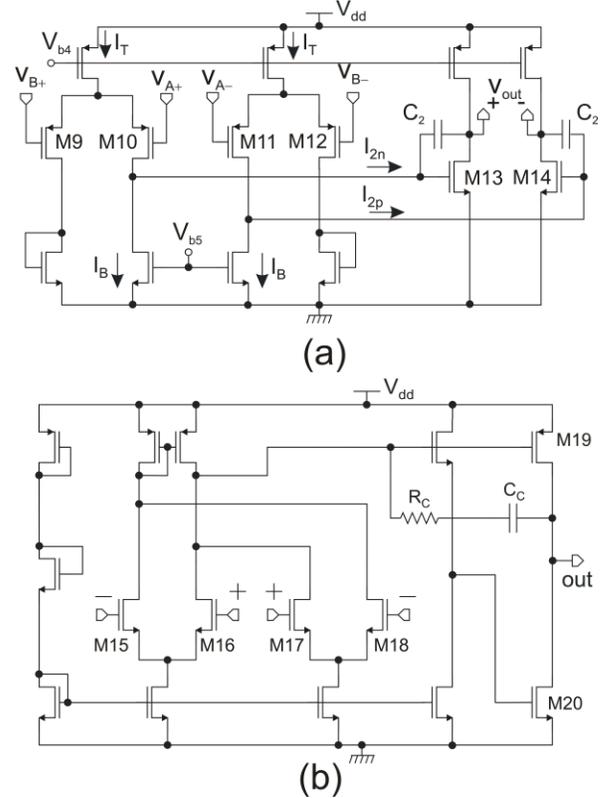


Fig.8 (a) complete INT2 schematic view; (b) CMDA architecture.

Finally, Fig.8 (b) shows the CMDA amplifier. The structure is that of a conventional two-stage op-amp, with duplicated input differential pairs. Inverting (-) and non-inverting (+) terminals are connected as in Fig.5. The class AB output stage provides enough impulsive current to drive the large input capacitance of the preamplifier in presence of fast input common mode transients. The bias chain on the left of Fig.8(b) provides a quiescent current that exhibits the proper dependence on V_{dd} required to obtain an acceptable PSSR from this kind of topology [28].

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The prototype was fabricated using the 0.32 μm , 3.3 V CMOS subset of the Bipolar-CMOS-DMOS BCD6s process (STMicroelectronics). The nominal DC gain ($A_0 = R_2/R_1$) was set to 200 and the target input noise density to 20 nV/sqrt(Hz) for a chopper frequency of 20 kHz. In order to obtain an effective ripple rejection, a cut off frequency $f_c = 200$ Hz with a Butterworth type response was chosen. The main parameters that appears in the block diagram of Fig.5 are summarized in Table I, while the dimensions of selected MOSFETs are reported in Table II. High resistivity polysilicon resistors are used in the feedback voltage divider, while all capacitors are of polysilicon/gate oxide/n-implant type. Chopper modulators S_{ps} and S_{smf} are implemented using complementary $p-n$ pass gates in order to maintain a low resistance over a wide voltage

range. Modulators S_{o1} and S_{o2} use only n -MOSFET and p -MOSFET, respectively. The size of S_{ps} devices, reported in Table II (same size for n and p MOSFETS), has been set to a value much larger than the minimum in order to reduce their thermal noise. A similar choice has been operated for the S_{mf} switches, but the reason here was to minimize the effect on the gain, since the switch series resistance adds up to R_{2A} and R_{2B} resistances. Simulations showed that the S_{mf} series resistance caused a gain increase of about 0.8 % with respect to the theoretical value (R_2/R_1).

OTA1 stage was designed considering the input noise voltage PSD at f_{ch} , as the main specification, since it sets the equivalent input noise voltage PSD in the baseband of the in-amp. The OTA1 input noise was equally distributed between contributions from G_{mB} and from the preamplifier.

TABLE I. MAIN DESIGN PARAMETERS

Parameter	Value
$A_1=G_{mA}/G_{mL}$	600
G_{mB}	33 nA/V
G_{m2}	190 nA/V
C_1	88 pF
C_2	107 pF
R_{1A}, R_{1B}	1k Ω
R_{2A}, R_{2B}	200 k Ω
I_0	42.5 μ A
I_2	0.94 μ A

TABLE II. DIMENSIONS OF SELECTED DEVICES

Device	W/L (μ m/ μ m)	Device	W/L (μ m/ μ m)
M1-4	6000/2	M13-14	6/6
M01-02	1/105	M15-18	5/24
M5-6	0.8/400	M19	312/9
M7-8	2/259	M20	39/5
M9-12	2/130	M23-24	4/85
M21-22	6/18	S_{ps} devices	30/0.5

The former contribution was controlled by using the relatively high pre-amplification gain reported in Table I. On the other hand, sizing of the preamplifier was aimed to make all contributions from devices other than the input MOSFETs negligible. Then, the input devices were pushed to deep subthreshold to optimize the g_m/I_D ratio and, consequently, the thermal noise vs. bias current tradeoff. This justifies the large M1-M4 aspect ratios reported in Table II. The non-minimum length was chosen to increase the device area and, consequently, reduce flicker noise contribution, which was not negligible even at the chopper frequency. More details on the heuristic approach adopted for the preamplifier design are reported in [16]. The clock signal was provided by an internal relaxation oscillator operating at $2f_{ch}$, followed by a frequency divider (a single T-type flip-flop). In this way, a clock at frequency f_{ch} and precise 50 % duty-cycle is obtained. An external resistor was used to tune the oscillator frequency.

An optical micrograph of the amplifier is shown in Fig.9, where the main blocks are specified. The circuit layout was aligned and superimposed on the actual micrograph to represent the circuit devices, otherwise hidden under planarization dummies. The total area occupied by the in-amp is 0.57 mm². The test chip includes also a clock generator and

other auxiliary circuits used for diagnostic purposes. These blocks are visible in the lower part of Fig.9.

The circuit operates with supply voltages in the range 2.7-3.6 V with a total current consumption of 170 μ A, including the oscillator. Most of this current is used by the preamplifier (60 %) and OP (24 %). The output common mode voltage was set to 1.4 V, to comply with the input range of G_{m2} transconductors. Unless differently specified, V_{CMI} was set to 1.4 V.

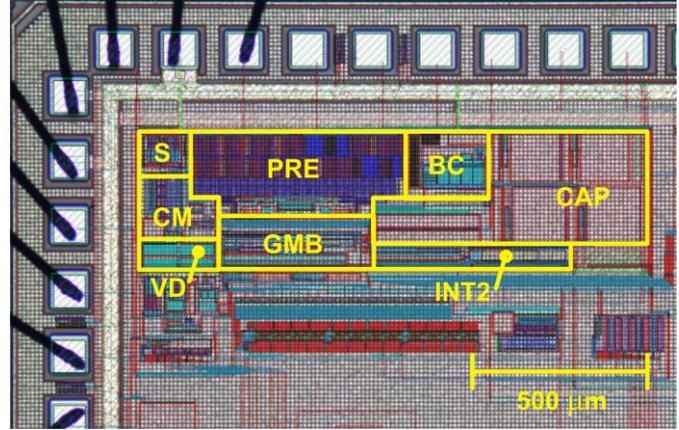


Fig.9. Photograph of the test chip area occupied by the in-amp. The chip layout is superimposed on the photo in order to represent the circuit devices, buried under the metal dummies. Blocks are as follows: S: S_{ps} ; switch array; CM: CMDA amplifier; PRE: preamplifier; GMB: Gmb transconductor, VD: feedback voltage divider (R_1, R_2), BC: Bias circuits; CAP: C_1 and C_2 capacitors.

The DC input-output characteristics have been measured using a parameter analyzer (HP 4145B). Frequency responses were acquired using a waveform generator (Agilent 33220A) and a 16 bit 2-channel digitizer (Pico Technology Ltd, mod. ADC216), both controlled by a personal computer. The same digitizer, combined with a programmable anti-alias filter, was used for noise measurements. A differential to single-ended (and vice versa) conversion board with calibrated attenuations was used to interface the mentioned instruments to the amplifier. All experiments were performed with $V_{dd}=3.3$ V and, unless differently specified, $V_{CMI}=V_{CMO}=1.4$ V, $f_{ch}=20$ kHz.

The output differential voltage is plotted in Fig.10 (a) as a function of the input differential voltage. The small signal gain, estimated by means of a linear fit in the $[-2$ mV, $+2$ mV] interval, is 201.2. The discrepancy with respect to the design value (200) is due to the mentioned effect of S_{mf} series resistance. The linearity error is less than 0.5 % of full scale in the interval of input voltages ± 10 mV, corresponding to an output swing of nearly ± 2 V. The linearity error is less than 500 ppm of full scale for $|v_{in}| < 5$ mV.

Fig.10 (b) shows the dependence of V_{CMO} on the input differential voltage, for various V_{CMI} values. The curves are practically coincident for V_{CMI} in the range 0.7-2.2 V. Lower or higher values alter the correct operation of the preamplifier. A significant dependence of V_{CMO} on the input differential voltage starting for $|v_{in}| > 5$ mV can also be observed. This phenomenon, which is identical for negative v_{in} values, occurs when the positive going output terminal exceeds the input

range of the corresponding p -differential pairs of INT2, disrupting the mechanism by which V_{CMO} tracks the output common mode voltage of the previous stage.

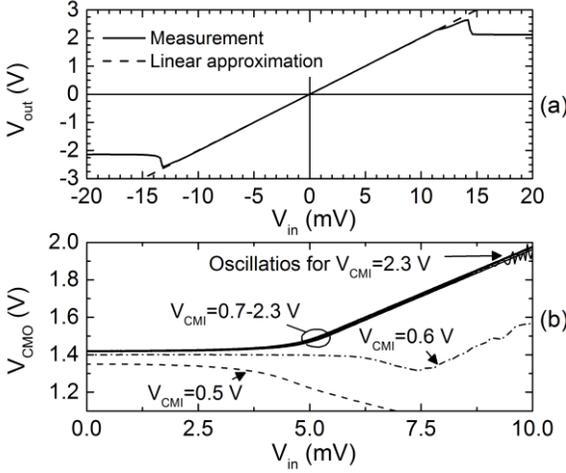


Fig.10. (a) Output differential voltage as a function of input differential voltage for $V_{CMI}=1.4$ V; (b) output common mode voltage as a function of input differential voltage for various V_{CMI} values.

Fig.11 shows the effect of V_{CMI} on the DC gain. The relative variation with respect to the value at $V_{CMI}=1.4$ fall within ± 0.2 % over a V_{CMI} interval even wider than that suggested for correct operation on the basis of Fig.10 (b).

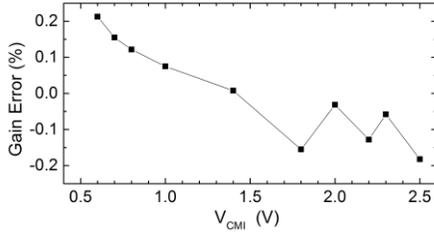


Fig.11 DC gain relative variation as a function of the input common mode voltage. The gain for $V_{CMI}=1.4$ V is taken as the reference.

Gain variations exceeding 50 % were observed in simulations performed over the same V_{CMI} range without common mode equalization. These variations were ascribed to the phenomenon illustrated in Fig.4 (b) and (c). The experimental result shown in Fig. 11 indirectly demonstrates the effectiveness of the input common mode equalization circuit. The relatively wide bandwidth of the input common mode equalization loop (325 kHz, from simulations) guarantees that the low sensitivity of the gain to the input common mode voltage is maintained even when the latter include large AC components. Experimental verification of this property was obtained by superimposing a large sinusoidal waveform (up to 600 mV peak-to-peak) on V_{CMI} while the input differential signal was set to 10 Hz, with magnitudes as large as to produce a peak-to-peak output voltage in the range 0.4-1 V. In these conditions, varying the frequency of the common mode signal up to 50 kHz did not produce significant differential mode gain variations, while intermodulation products were more than 60 dB below the output main tone (10 Hz).

The amplifier magnitude and phase frequency response is shown in Fig.12 (a) and 12 (b), respectively. The response was acquired for different values of the source resistance (R_S), simply implemented by means of two identical resistors of value $R_S/2$ placed in series to each input terminal (balanced configuration). The curve for $R_S=0$ shows a slight difference with respect to the ideal Butterworth behavior. This discrepancy, which is clearly not critical for the performance of the amplifier, is probably due to the relatively high sensitivity of ω_0 and Q to process variations.

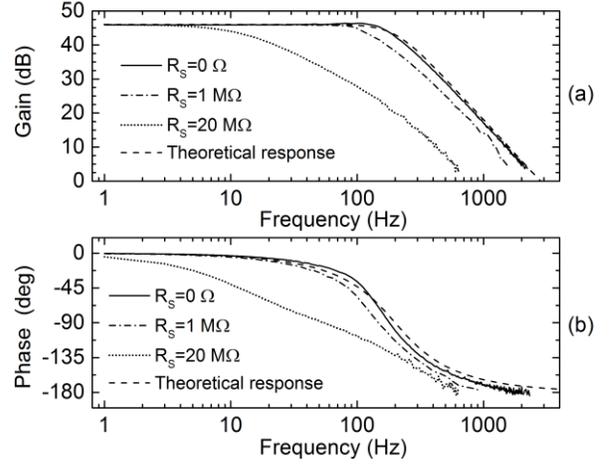


Fig.12 Magnitude (a) and phase (b) response of the amplifier with different signal source resistances (R_S), compared with the ideal 2-nd order low pass Butterworth response. .

A more interesting feature is the dependence of the magnitude on the source resistance. At low frequencies, all curves converge to the same asymptotic value. Considering that the preamplifier input capacitance is 14 pF (estimated by AC simulations), with a conventional chopper ICF architecture the effective input resistance for $f_{ch}=20$ kHz would have been around 890 k Ω . This value, combined with $R_S=20$ M Ω , would result in an attenuation of nearly 27 dB, which is apparently not visible in Fig.12. This demonstrates the beneficial effect of the proposed SCPS approach on the input resistance. A deeper insight into this point was obtained by estimating the input impedance from the data of Fig.12, using the following equation for the input attenuation:

$$\frac{(v_{out}/v_s)_{R_S=R}}{(v_{out}/v_s)_{R_S=0}} = \frac{Z_{in}}{R + Z_{in}} \quad (27)$$

where R_S is the generic output resistance of the signal source and $R=20$ M Ω . The results (experimental points) are presented in Fig.13 (a) for two chopper frequencies. The magnitude of Z_{in} is compared with theoretical prediction calculated using (4) with $C_p=14$ pF and a fit of the experimental response for $H(f)$. A good agreement between experimental and theoretical data can be observed. As the frequency increases, the Z_{IN} boosting factor progressively decreases, producing the excess attenuation and phase delay visible in Fig.12 for $R_S \neq 0$. Fig.13 (b) shows the maximum relative difference between Z_{in} measurements performed on three different samples.

Differences are smaller than 10 % across nearly the whole amplifier passband, demonstrating the robustness of the resistance boosting approach.

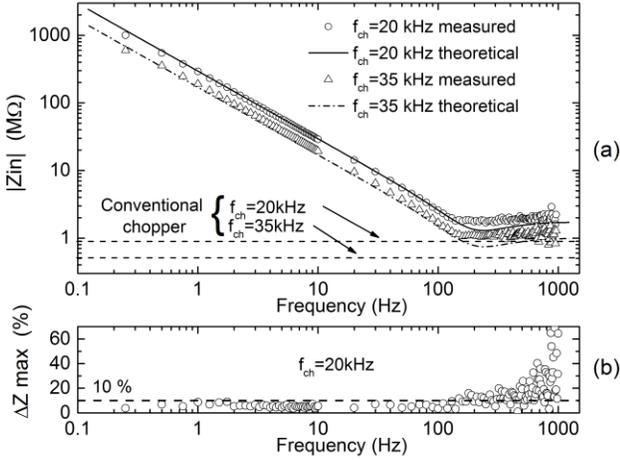


Fig 13. (a) Magnitude of the input impedance: measurements (points) and theoretical behavior (lines) for two chopper frequencies. The input resistances that would have been obtained with a conventional chopper amplifier and same input capacitances are indicated by the horizontal lines. (b) Maximum relative difference (absolute value) measured over input resistance measurements performed over a set of three different samples.

The output noise spectral density is shown in Fig.14 for three different source resistances. Considering the case for $R_S=0$, the flat region in the amplifier passband corresponds to an input referred noise voltage of 18 nV/sqrt(Hz), while the flicker corner frequency is around 0.2 Hz. The spectral density measured for $R_S=40$ MΩ exhibits a considerable excess noise that has been ascribed to the contribution of the input bias currents due to charge injection from the input modulators [29]. The average DC value of the bias currents was 300 pA, with an offset component around 50 pA. The estimated bias current noise density was 60 fA/sqrt(Hz). Current noise contribution is negligible for the case $R_S= 1$ MΩ.

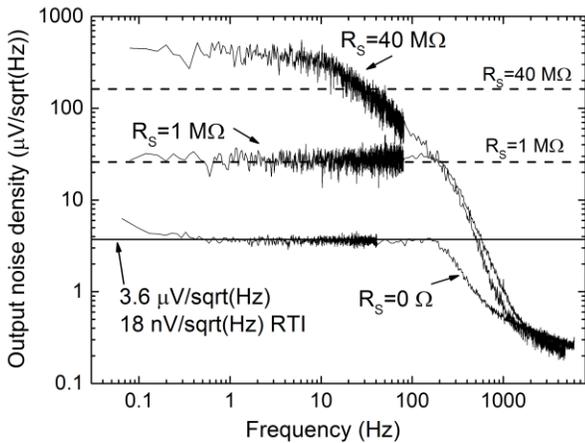


Fig 14. Output noise voltage spectral density measured with three different input source resistances, indicated for each curve Dashed lines represent the passband noise contribution from only the source resistance, for the cases $R_S=1$ MΩ and 40 MΩ. The background noise of the noise measurement set-up was less than 30 nV/sqrt(Hz) over the whole displayed frequency range.

Periodical AC Noise simulations revealed that the visible residual flicker noise contribution originates from devices M21-24 of the G_{mb} transconductor, which, as already stated, are not affected by chopper modulation. The slope change occurring at high frequencies can be understood considering that, for $f > f_c$, H_{BP} decreases with half the slope of H_{LP} , making INT2 contribution dominant in the upper frequency interval. This explanation is supported by simulations presented in [15]. The Total Harmonic Distortion (THD) is shown in Fig.15 as a function of the input amplitude. At frequencies much lower than f_c , distortion keeps below 1 % even for input levels exceeding the 5 mV limit (10 mV_{p-p}), set by the V_{CMO} control mechanism. Distortion get worse as the frequency increases, as shown by the 90 Hz curve, where the 1 % THD level is crossed with just a 5 mV_{p-p} input stimulus. The distortion increase with frequency occurs when, due to the H_{LP} response, the feedback signal does not effectively compensate the input signal and the preamplifier output voltage increases, exceeding its maximum swing. Mitigation of this effect could be obtained by reducing the pre-amplifier gain at the cost of a less area-efficient implementation of INT1 [15].

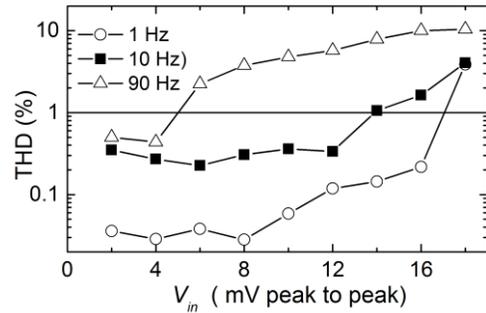


Fig 15. Total Harmonic Distortion (THD) as a function of input signal peak-to-peak amplitude for three different frequencies.

Table III shows a list of specifications of the proposed amplifier, compared with five recent works. The total output ripple was estimated summing up the contribution of the first three harmonics of f_{ch} . The input referred ripple reported in the table is obtained by dividing the output ripple magnitude by the passband gain A_0 . The input offset voltage and gain standard deviations have been estimated over a set of 5 samples. Measurements performed varying the temperature over a 20 °C-100 °C interval with a Peltier Cell cryostat showed that the total average offset drift was 5 nV/°C, while the DC gain drift was 12.5 ppm / °C.

Among the amplifiers included in table III, the proposed architecture exhibits the highest input resistance. Input resistance data are not provided in [25] and [26], but both use a standard configuration for the chopper modulators, so that an input resistance not exceeding a few tens of MΩ can be expected. The relatively high input resistance reported in [30], is obtained by pre-charging the input capacitance with a buffered version of the input signal before each chopper transition. This very simple approach may introduce offset and 1/f noise contributions from the buffers, even with pre-charging times much smaller than the chopper period. This is proven by the relatively high flicker corner reported in [30], which can become a critical point when trying to reduce the

input noise density to levels similar to the other amplifier in the table. The input noise vs. supply current tradeoff obtained with the proposed circuit and expressed through the noise efficiency factor (NEF) is comparable to architecture of similar complexity [14], [21]. Better NEF and area occupations figures are obtained by means of a simpler architecture [26], which, on the other hand, shows less effective ripple rejection and lacks both DEM and input resistance boosting functions.

V. CONCLUSIONS

We have shown that alternating the input and feedback port of an ICF amplifier at the same frequency as chopper modulation produces a dramatic increase of the switched-capacitor parasitic input resistance associated to the input chopper modulator. The proposed approach has been applied to a modified ICF chopper in-amp capable of self-filtering all

ripple contributions exploiting its second order low-pass transfer function. The amplifier embodies a feedback loop that equalizes the input and feedback common mode voltages, which is a prerequisite for the application of the proposed resistance boosting approach. Measurements performed on the prototype showed that the input impedance is increased by more than two orders of magnitude for frequencies two decades below the amplifier cut-off frequency. This makes the amplifier particularly interesting for interfacing sensors having small bandwidths, which is a frequent condition with a large variety of MEMS sensors. In these cases, the low cut-off frequency of the amplifier acts as an anti-alias filter for the typically wide noise bandwidth of the sensors, allowing direct connection to a low sampling-rate ADC. The amplifier is also sufficiently compact to be integrated into relatively small systems on a chip.

TABLE III. AMPLIFIER SPECIFICATIONS COMPARED WITH STATE OF ART.

Parameter	This work	[14]	[21]	[25]	[26]	[30]
CMOS Process	0.32 μm	0.7 μm	0.7 μm	0.5 μm	0.13	40 nm
DC gain	201.2	100	100	1000	1000	40
Gain drift	12 ppm/ $^{\circ}\text{C}$	3 ppm/ $^{\circ}\text{C}$	NA	NA	405 ppm/ $^{\circ}\text{C}$	NA
GBW	40 kHz	900 kHz	900 kHz	800 kHz	32 MHz	200 kHz
Input noise density	18nV $\sqrt{\text{Hz}}$	17 nV $\sqrt{\text{Hz}}$	21 nV $\sqrt{\text{Hz}}$	27 nV $\sqrt{\text{Hz}}$	13.5 nV $\sqrt{\text{Hz}}$	100 nV $\sqrt{\text{Hz}}$
1/f corner	0.2 Hz	1mHz	1 Hz	<0.1 Hz	NA	>50 Hz
CMRR	> 120 dB	127 dB	137 dB	142 dB	102 dB	NA
PSSR	115 dB	130 dB	120 dB	138 dB	101 dB	NA
Input referred ripple (rms)	0.2 μV	0.87 μV	0.39 μV	NA	72 μV	NA
Input offset voltage	2 μV	< 3 μV	< 2 μV	2.8 μV	3.5 μV	NA
Input offset drift	5 nV/ $^{\circ}\text{C}$	15 nV/ $^{\circ}\text{C}$	22.5 nV/ $^{\circ}\text{C}$	3 nV/ $^{\circ}\text{C}$	25 nV/ $^{\circ}\text{C}$	NA
Gain error	$\pm 0.3\%$	0.06 %	0.53 %	$\pm 0.1\%$	NA	NA
Rin	> 1 G Ω	26 M Ω	< 7 M Ω	NA	NA	300 M Ω
Area	0.57 mm ²	5 mm ²	1.8 mm ²	2.5 mm ²	0.06 mm ²	0.071 mm ²
V _{supply}	3.3 V	5 V	5 V	3-5.5 V	1.5 V	1.2 V
I _{supply}	170 μA	290 μA	143 μA	1.7 mA	194 μA	1.66 μA
NEF	10.6	11.2	9.6	43	7.2	4.9

ACKNOWLEDGMENT

The authors wish to thank STMicroelectronics for fabricating the test chip described in this work.

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